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CHARGE DOMAIN FILTERS FOR ENHANCED MONOLITHIC SIGNAL PROCESSING

General Electric Company

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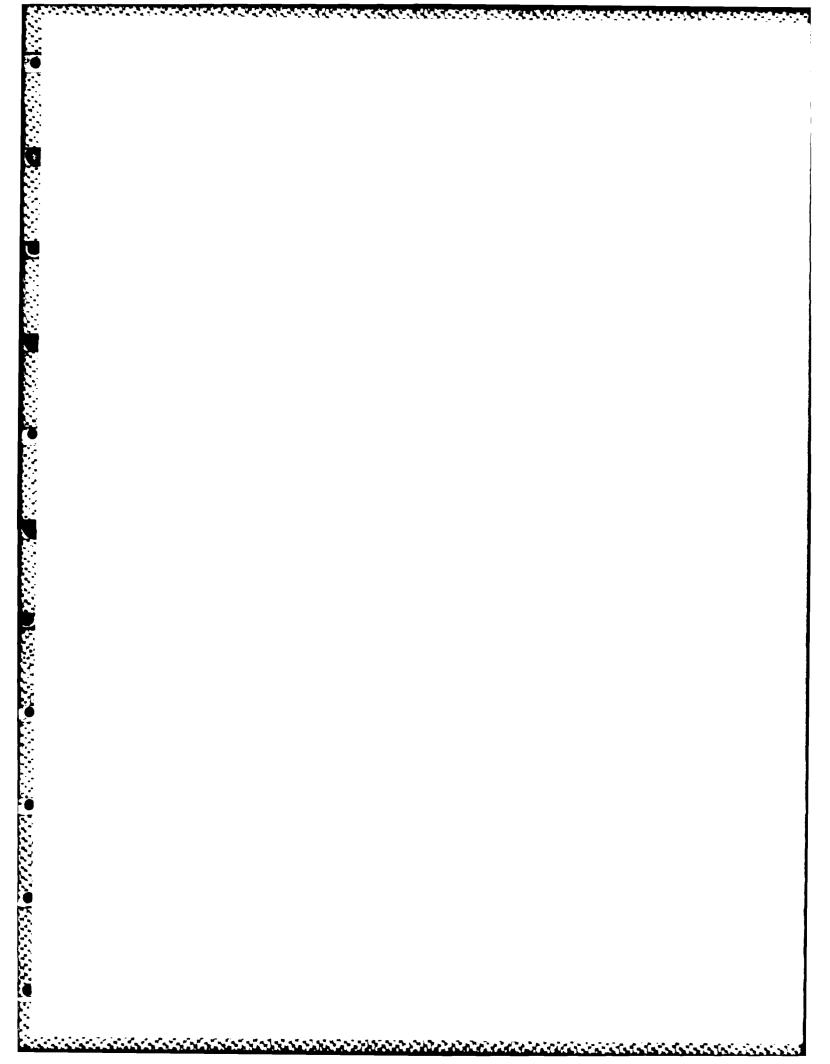
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CHARGE DOMAIN FILTERS FOR ENHANCED MONOLITHIC SIGNAL PROCESSING

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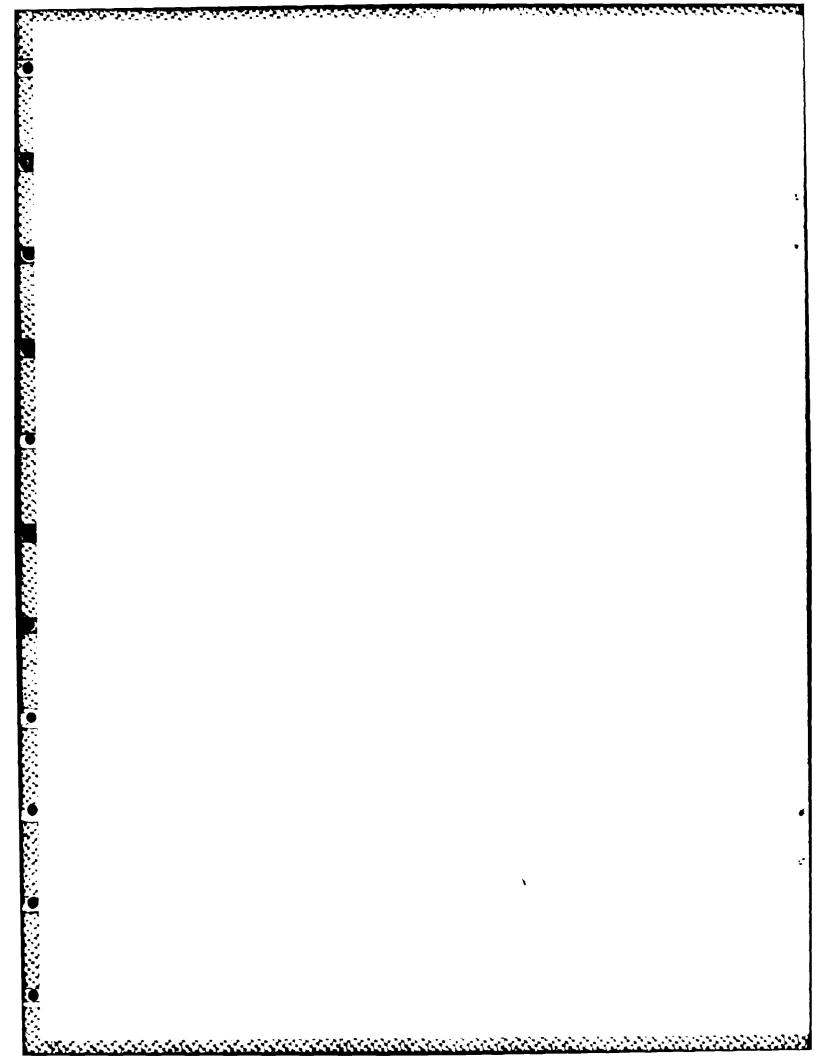
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The Charge Domain Device (CDD) concept in sampled analog signal processing on a chip has been investigated both theoretically and experimentally under this contract. The basic operations required for signal processing functions have been evaluated, and new structures have been discovered which yield an improved level of design flexibility. The physical limitations of the charge domain approach and their effect on overall device performance have been determined. In addition to numerous test structures, which were fabricated to evaluate new and improved device structures, design methodologies and tools useful for both mathematical design and structural optimization were also been developed. An 8-pole narrowband bandpass filter has been designed, fabricated and tested in order to demonstrate the wide range of capabilities of charge domain devices. The experimental characteristics of a filter having a bandwidth of 1/100 of the clocking frequency and over 65 dB passband-to-stopband ratio exemplify these characteristics and verify the utility of the design tools of the program. Design concepts for digital control of filter coefficients' - an

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initial goal – have, also been developed.   This permits a single generic chip type to be used
in a large number of applications and opens the door for applications requiring high speed
adaptive processes.   Test chips have been fabricated and evaluated which demonstrate these
concepts.

Further capabilities of charge domain filters are discussed and several applications
examples for this technology are described.   The potential now exists for incorporating
higher performance, higher speed signal processing systems on a chip.
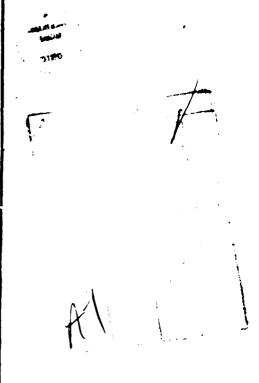
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FOREWORD

This Final Report was prepared by GE Corporate Research and Development, Schenectady, NY, under Contract F19628-80-C-0213. Dr. Sven Roosild of Defense Advanced Research Projects Agency and Dr. Freeman Shepherd of Rome Air Development Center East were Project Scientists, and Dr. Paul Pellegrini also of Rome Air Development Center East was Contract Monitor. The report covers work conducted from October 1, 1980 through May 31, 1983 in the Electronics Laboratories, Dr. Kenneth Pickar, Manager; Dr. J.J. Tiemann was the principal investigator. Contributors to the research described herein and to this report included Dr. J.J. Tiemann and Mr. T.L. Vogelsong of the Corporate Research and Development Center and Dr. A.J. Steckl and Mr. S. Bencuya of the Electrical Engineering Department of RPI.

I. INTRODUCTION

A new class of integrated circuits, called charge domain devices (CDD) has been developed with the goal of performing signal processing functions with accuracy and speed performance exceeding alternative technologies. The starting point for this development is conventional charge transfer device (CTD) technology.[1] Devices of this type such as charge coupled device (CCD) transversal filters[2,3] have been demonstrated in many cases, particularly at high frequencies, to be more efficient in performing particular sampled data processing functions than such alternative techniques as digital filters or switched capacitor devices. However, as the speed and accuracy performance requirements increase, conventional CTD's also encounter a number of limitations, and it is the purpose of the development effort covered in this report to provide a technology which permits higher speed operation and wider dynamic range by avoiding these limitations. In order to understand the origin of some of these limitations, the operation of conventional CTDs are briefly reviewed.

Conventional CTD's derive their output signal by sensing charge packets with overlying MOS electrodes. Multiplication of these charges by tap weights is implemented by splitting the overlying electrodes in proportion to the desired impulse response coefficient, and summation is implemented by connecting the overlying electrodes. This implementation is particularly efficient, since all of the mathematical operations are accomplished automatically by simple physical laws rather than by manipulating binary bits in complex logic circuits, but it causes at least two of the problems. First, as the specifications on the system increase, and the number of filter coefficients needed to accomplish the desired transfer function increases, the total capacitance of the output electrode increases, making high speed operation more difficult; and second, non-linearities in the relationship between the charge in the packets and the voltage induced on the overlying electrodes usually compromises the accuracy of the transfer function if buried channel technology is used. These constraints have in the past limited the frequency handling capabilities of conventional CTD filters to a few megahertz.

Charge domain integrated circuits have been developed to overcome these limitations so as to increase the frequency range that can be handled by monolithic signal processing chips.[4,5] In charge domain devices, all signal processing is performed by manipulating the charge packets themselves, rather than using the image charge on overlying electrodes. The charge packets representing the input signal may be split, routed, delayed and combined to form new charge packets that represent the output signal. But since the splitting and routing depend only on the plan view geometry of the devices that accomplish it, and not on the details of the capacitance-voltage characteristic, buried channel technology can be used without degrading the accuracy of the transfer function. Furthermore, since portions of some charge packets can be routed backwards in the signal flow sense and re-introduced into the forward path, CDDs yield the new possibility of filters with infinite impulse response; i.e., filters that implement poles as well as zeroes in their transfer function. Finally, since the output of these devices is a stream of charge packets, low capacitance diode sensing of the charge is used to generate the output signal. Thus, the output capacitance does not increase as the filter architecture becomes more complex, and device speed is limited only by the speed of charge transfer which, for buried channel technology, may be as large as hundreds of megahertz.

The purpose of this contractual effort was to investigate the unique capabilities of charge domain devices and to develop them for high speed sampled data analog signal processing. Specifically the three goals of the contract are, as stated in the original proposal:[6]

- To investigate the fundamental physical operation and limitations of the charge domain concept and the relationship to analog filter performance characteristics. This will cover the relationship between such device characteristics as lateral transfer speed, charge packet splitting accuracy, and such performance characteristics as filter accuracy, linearity, and bandwidth.

- To design and implement a charge domain filter as a test vehicle that will demonstrate performance capabilities for a selected application. The filter's design will include the full range of trade-offs between poles and zeros, a unique feature of the charge domain concept.

- To investigate the feasibility of introducing programmability into charge domain filters. Basic programmable building blocks will be designed, fabricated, and evaluated as part of this program. It is envisioned that the results of this work will lead to a future program to produce a digitally programmable

mable filter module controlled by readily available microprocessors. In this fashion, future signal processing building blocks can be implemented with software configurability and thus quickly and conveniently integrated into a variety of applications.

This investigation has covered all the areas outlined in the proposal and has gone into more depth in several of the areas. The goals of the contract have been addressed, and the successful demonstration of design methodologies, test vehicle filters and programmability concepts has proven that the charge domain concept is indeed a powerful new technique for flexible realizing signal processing functions, and ultimately entire systems on a single integrated circuit chip.

Section 2 discusses some of the basic charge domain operations for delay, multiplication and addition. Section 3 describes the representation of signals in the charge domain which permits four quadrant arithmetic functions to be realized. Also in this section is a description of the mathematics underlying a filter design. This leads into Section 4 which details some of the device structures which are needed to implement the mathematical functions and their capabilities and limitations. Several charge domain structures which overcome these limitations are described in Section 5.

Section 6 discusses performance characteristics such as linearity, dynamic range and bandwidth. The operation of charge splitting, which determines coefficient accuracy is also discussed. The physics of this operation has been investigated through testing of structures. These results indicate experimentally how the splitting structure may be optimized for accuracy.

Section 7 describes computerized test stations which have been developed for data acquisition to characterize the accuracy and noise levels of charge domain devices. Experimental results, which are much more precise than those obtained by previous methods, are also presented.

Section 8 discusses the computer aided filter design tools which have been developed as the work proceeded. These tools are used in the interpretation of the test results and also in determining the feasibility of certain filter designs prior to device fabrication.

Section 9 details the actual design and operation of two charge domain filters which have been developed for this contract, a simple three pole low pass filter, and an eight pole narrowband bandpass filter. Both of these filters have been successfully demonstrated and experimental measurements of their performance are included.

As mentioned above, one of the major goals of this contract is to provide the capability of electrically programming the coefficients that characterize the transfer function of a CDD filter. Section 10 describes several approaches which can be taken to realize digitally programmable devices. Two of these, namely a sequential method which minimizes chip area and a pipelined method which optimizes speed, have been successfully implemented, and experimental results are presented.
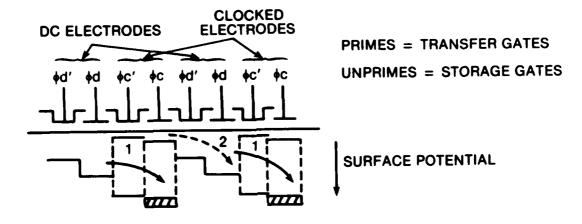
Section 11 looks to the future and describes other features of the charge domain which have not yet been utilized. This section describes some applications which could be efficiently addressed with charge domain technology and would eventually result in the desired system on a chip. All of the results to date, and possible future extensions are summarized in Section 12.

2. BASIC CHARGE DOMAIN OPERATIONS

Discrete time signal processing requires only a relatively small number of functions; namely, delay (memory), and four quadrant addition and multiplication. In order to optimize performance, these functions must be implemented over a wide dynamic range, yet consume little power and silicon area. This section describes how the charge domain concept addresses these requirements.

2.1 INTACT CHARGE PACKET TRANSFER

Charge packet transfer is the basic operation used in both the CCD delay line and the CCD split electrode transversal filter. It can be accomplished in a number of different ways.[1,8] The technique used for this contract is the pseudo one phase approach shown in top-view and cross-section in Figure 2.1. This technique requires 4 electrodes per stage. A 50% duty cycle clock is applied to the two electrodes in the center of Figure 2.1. These electrodes are called, respectively, the clocked transfer electrode and the clocked storage electrode. The other two electrodes are held at DC, and are called
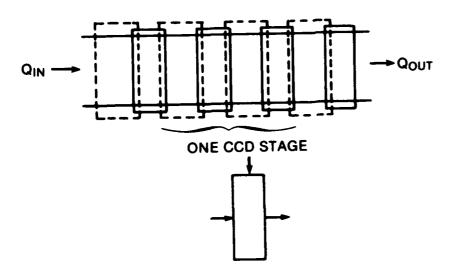
Figure 2.1. Pseudo one phase CCD operation.

the DC transfer electrode and the DC electrode storage, respectively. When the clock lines are turned on the ... into ... charge packet transfers to the region under the clocked storage gate as shown. When the clock turns off, the charge packet transfers to the right underneath the DC storage electrode. Thus there is one full stage of transfer per one full clock cycle (one delay period). As a shorthand notation for other figures, one full stage including four electrodes is shown schematically as a single rectangle representing the plan view of the reservoir holding the charge during one of the clock phases.

2.2 PACKET SPLITTING

As shown in Figure 2.2, this operation is identical to the basic operation described above except that the receiving reservoir is comprised of two or more sections whose total capacitance is roughly equal to that of the source reservoir, but whose relative sizes correspond to predetermined ratios. Once the charge has been split into portions, each individual portion can be manipulated independently. This unilateral splitting action can be conveniently obtained by starting the leading edges of the barrier regions that separate the receiving reservoirs in the transfer gate region of the shift register structure as shown in the Figure. If the potential in the transfer gate region is always higher than the receiving

$$Q_1 + Q_2 + \cdots + Q_N = Q$$

$$\frac{C_1}{\Sigma C_i} = \frac{Q_1}{Q} \text{ , etc.}$$

ION IMPLANT OR THICK OXIDE

SPLIT TAKES PLACE IN REGION OF CHARGE FLOW: UNILATERAL
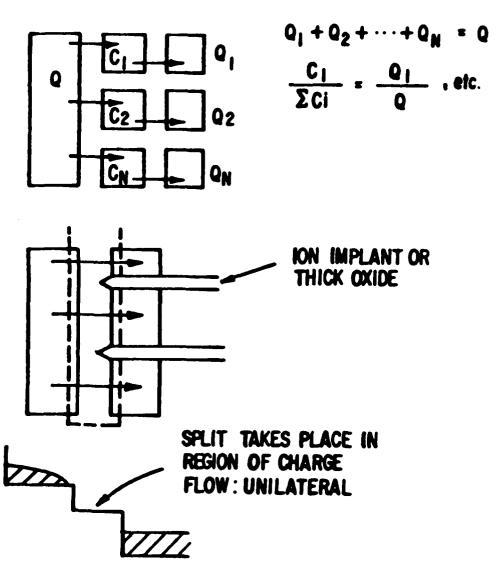
Figure 2.2.   Barrier charge packet splitting.

reservoirs, the charge will not be able to "back up" around the barriers between the reservoirs. Although the leading edges of the barriers are shown coming to a point, this feature is not essential. It is helpful, however, in minimizing the effect of small, uncontrolled electric fields on the division of the total charge among the receiving reservoirs.

The packet splitting operation described above is used to implement multiplication, but some problems must be faced. First of all, it is not be possible to implement coefficients greater than unity with this approach, and second, the implementation of multiplication by a negative number is not obvious. Both of these points are addressed in detail later.

2.3 PACKET COMBINING

As can be seen in Figure 2.3, this operation is also essentially identical to the basic transfer operation discussed above. This time several component packets are simultaneously transferred into a single reservoir, and it is obvious that this operation implements the summation of the individual component charge packets.

2.4 EQUILIBRATION

A technique called "equilibration" is used to implement both addition and multiplication in a single step. In this operation, which is shown in Figure 2.4, two charge storage regions are briefly connected together during each clock period by turning on the equilibration gate that separates them. During the time this gate is open, charge flows between the reservoirs so as to equalize their potentials. After equilibration, the gate is turned off, leaving amounts of charge in each reservoir in proportion to their respective capacitance (assuming equal applied voltages and threshold voltages) irrespective of the initial distribution of charge. Since charge is required to move in both the X and Y directions in this structure, there is a potential speed problem. The relatively long time required for an initially unequal charge distribution to become uniformly distributed can be greatly reduced by introducing a lateral diffusion channel to lower the lateral resistance and thereby reduce the time constant. This diffusion may be overlayed by a metal to further enhance lateral transfer speed. The penalty inherent with this technique, which results in a structure similar to a stage in a bucket brigade delay line, is higher transfer loss. However, since only a small number of these stages are required in a device, this is usually not a limitation.

$$Q = Q_1 + Q_2$$
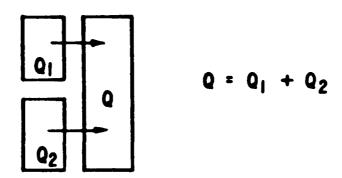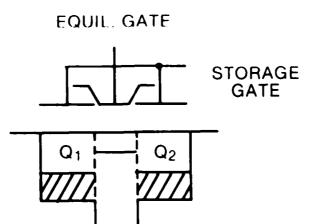
Figure 2.3. Charge package summation.

EQUIL. GATE

STORAGE
GATE

Q₁   Q₂

A₁

EQUIL. GATE

A₂
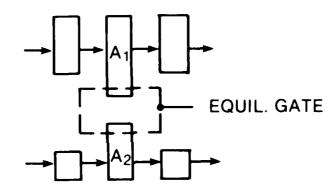
Figure 2.4.   Gated equilibration charge splitting.

3. SIGNAL PROCESSING

3.1 SIGNAL REPRESENTATION

For general filter design, it is necessary to represent positive and negative impulse response coefficients as well as positive and negative signal values, and it is necessary to implement multiplication correctly in all four quadrants. Although representation of positive and negative signal values can be accomplished in the charge domain by the use of a bias charge, it is more convenient to use two separate charge packets for each signal sample. In this case, the actual signal level can be represented by the difference between these two charge packets. This approach has the advantage that the zero level is not required to be fixed, but can be at any level; all that is required to represent a zero signal level is that the two packets be equal to each other. Thus, all of the signal processing elements which are described have two input charge packets for each signal sample, and they will produce two output charge packets. The output signal sample is represented by the difference between the charges in these output packets without regard to their absolute values. Thus, these output packets are in the exact same format as the input packets, and can be fed into another signal processing element directly to implement the cascade of the processes. A differential amplifier is required to produce the final output signal, but no amplifiers are needed at any intermediate point in the structure. This representation provides the additional benefit of rejecting common mode interference at the output such as feedthrough of clock waveforms, dark current, and other undesired signals.

Packet splitting is used to implement multiplication. Positive co-efficients (less than unity) are implemented by delivering the desired fraction of each packet to the corresponding output packet, and negative coefficients (less than unity) are implemented by delivering the selected portions to the opposite polarity output packet. It is easy to show that this scheme does indeed implement four quadrant multiplication correctly. (Note that a negative signal is represented by a larger negative charge packet and that this is delivered to the positive output when the coefficient is negative. Thus, a negative signal multiplied by a negative coefficient results in a positive output.)

3.2 IMPLEMENTATION OF MATHEMATICS

A general form of the difference equation that is to be implemented by the filter is
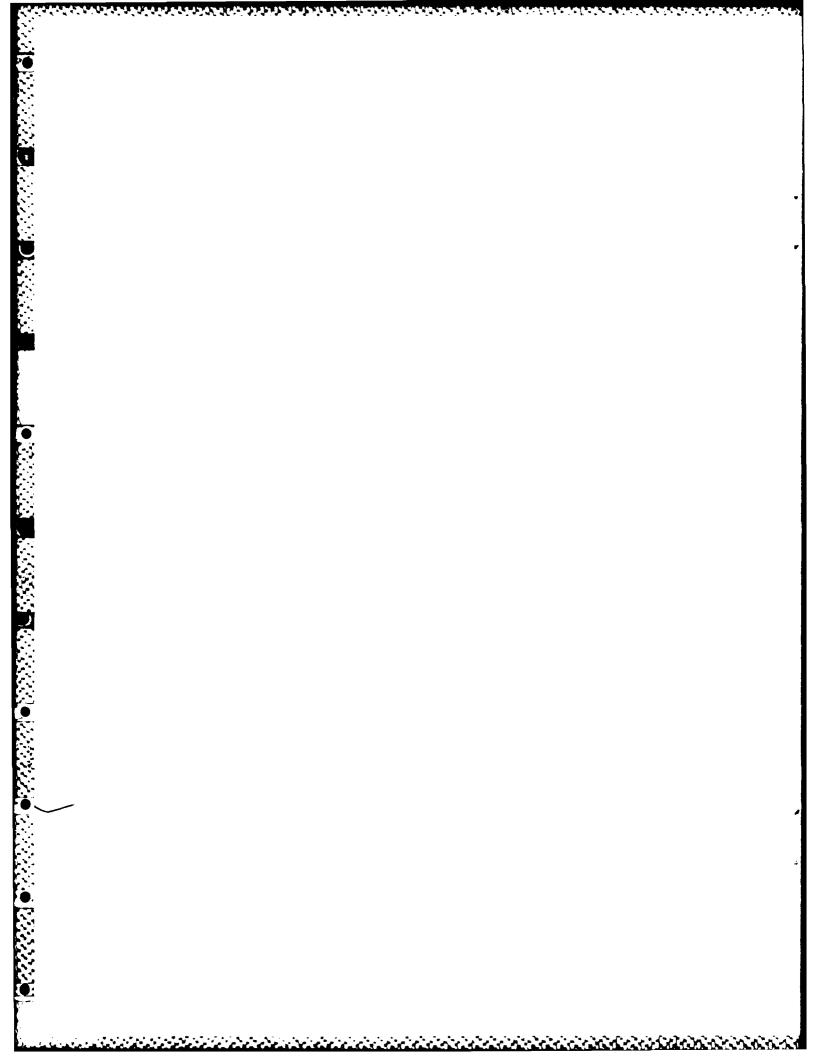
$$Y_n = \sum_{k=1}^{N} A_k Y_{n-k} + \sum_{k=0}^{M} B_k X_{n-k} \tag{3.1}$$

and the corresponding transfer function for the Z-transform is

$$H(Z) = \frac{\sum_{k=0}^{M} B_k Z^k}{1 - \sum_{k=1}^{N} A_k Z^k} \tag{3.2}$$

The poles of the transfer function are the roots of the polynomial in the denominator, while the zeros are the roots of the numerator in Equation (3.2).

To keep the physical implementation simple, we restrict the coefficients to real numbers. It is often useful to consider the denominator as a product of first and second order factors having real coefficients. Since the original rational transfer function can be implemented as a cascade of individual factors or as a sum of partial fractions, it is only necessary to discuss the implementation of one first order and one second order factor. Although the numerator can also be factored in a similar manner, it is usually practical to implement several zeros at once by using transversal filters of modest length. Thus, it will not be necessary to deal with the elementary factors in the numerator. Also, note that numerator coefficients can always be scaled such that their sum is unity, and that the only effect is a change in the overall gain. Unfortunately, the same cannot be said for the denominator. The unit term in the denominator of equation (3.2) came from the left hand side of equation (3.1), and this term sets the scale for the A's. Furthermore, most of the desirable pole locations involve second order factors in which the coefficient of the first order term has a magnitude greater than unity. Since it is impossible to implement such coefficients in a purely charge domain design, it has long been thought that these poles cannot be implemented without resorting to devices that provide active gain.

4. GENERAL APPLICATION REQUIREMENTS

The charge domain basic building block functions can be connected just as the sections of a block diagram of a sampled data filter are connected in order to provide for the poles and zeroes of the filter's transfer function. There are limitations on the placement of the poles and zeroes due to the constraint of having no gain elements in the system and of performing only fractional multiplications. The real axis pole corresponds to an exponential decay in the time domain, while the complex pole pair corresponds to a decaying sine wave.

The desired transfer function for a real axis pole is

$$H(Z) = \frac{k_1}{(Z - \alpha_1)} = \frac{k_1 Z^{-1}}{1 - \alpha_1 Z^{-1}} \tag{4.1}$$

and so the pole is placed at $Z = \alpha_1$. The Z^{-1} term in the numerator of Equation 4.1 only provides unnecessary delay of the output. Removal of this delay by placing a zero at the origin ($Z = 0$) will provide a smaller CDF structure and reduce the throughput delay. The resulting difference equation is

$$Y(Z) = \alpha_1 Z^{-1} Y(Z) + k_1 X(Z) . \tag{4.2}$$

The block diagram for this function is shown in Figure 4.1. By varying α_1 from zero to one or zero to minus one, the pole can be placed anywhere on the real axis within the unit circle ($-1 < Z < 1$). At the split the sum of the magnitudes of the coefficients must be less than or equal to one so the maximum gain is when $k = 1 - |\alpha_1|$. This gain constraint can be compensated for by proper sizing of the adjacent circuitry. Thus implementation of a pole on the real axis is realizable within charge domain constraints.

The transfer function of the complex pole pair is

$$H(z) = \frac{k_2}{z^2 - 2a_2z + (\alpha_2^2 + w_2^2)} = \frac{k_2 Z^{-2}}{1 - 2\alpha_2 Z^{-1} + (\alpha_2^2 + w_2^2)Z^{-2}} \tag{4.3}$$

thus placing poles at $Z = \alpha_2 \pm jw_2$. The Z^{-2} term in the numerator can be removed with a second order zero at the origin. The resulting difference equation is

$$Y(Z) = k_2 X(Z) + 2\alpha_2 Z^{-1} Y(Z) - (\alpha_2^2 + w_2^2)Z^{-2} Y(Z) . \tag{4.4}$$

Its block diagram is given in Figure 4.2. In this case the sum of the required coefficient magnitudes at the split may become greater than one even for $k_2 = 0$ for certain pole locations. The realizable pole locations for direct charge domain implementation of a second order section are inside of the dashed lies of Figure 4.3. This imposes a severe limit on design flexibility since many of the desired poles are outside of this region.

The solution is to find functions which can be implemented in the charge domain which provide poles in their desired locations plus some other non-desired poles. The spurious poles may be cancelled
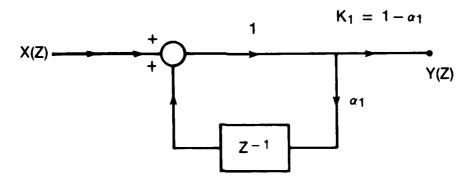
Figure 4.1. Recursive accumulator block diagram
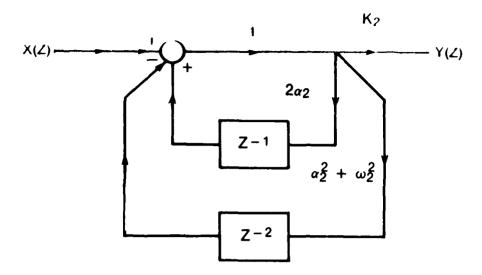
Figure 4.2. Complex pole pair block diagram.
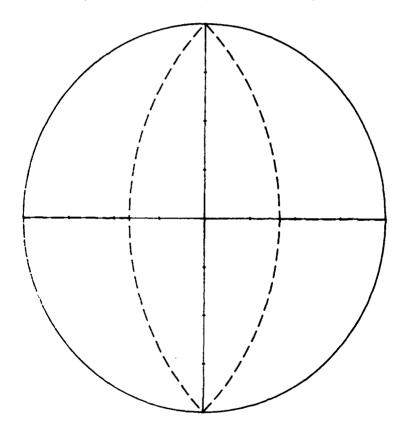
Figure 4.3. Allowable pole locations (inside the dashed lines) with a second order section in charge domain technology.

out with zeroes which can be placed anywhere in the z-plane by using a charge domain transversal filter. One such function is

$$H_1(Z) = \frac{k_2}{(Z^N + \lambda)} = \frac{k_2 Z^{-N}}{1 + \lambda Z^{-N}} . \tag{4-5}$$

The associated difference equation (assuming the addition of an Nth order zero at the origin) is

$$Y(Z) = k_2 X(Z) - \lambda Z^{-N} Y(Z) \tag{4-6}$$

where $k_2 = 1 - \lambda$. The block diagram of a recursive resonator which implements this function in shown in Figure 4.4. The roots of this equation are

$$Z = (-\lambda)^{n/N} \quad n = 1, 2, \cdots N \tag{4-7}$$

which yield N poles equally spaced around the unit circle. In polar coordinates the poles are located at

$$Z = \alpha^N \exp[i(2n-1)\pi/2N] \tag{4-8}$$

For example, with $N = 5$, $\lambda = 0.2$ and $k_2 = 0.8$, the poles are located as shown in Figure 4.5. If one is allowed to freely choose N and λ, poles can be placed anywhere within the unit circle. Note that it is impossible to build an unstable filter in the charge domain because the magnitude of the coefficient α is limited to less than one by lack of gain elements in the circuit and the conservation of charge at the splitting junction. Normally, one is interested only in a small number of the pole pairs produced by the structure shown above, and the unwanted poles must be canceled by a transversal filter. When the zeroes implemented by the transversal filter are placed directly on top of the unwanted poles, the desired transfer function is obtained.

$$k_2 = 1 - \lambda$$
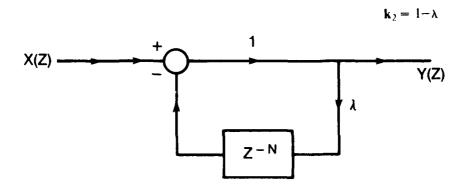
Figure 4.4. Recursive resonator block diagram.
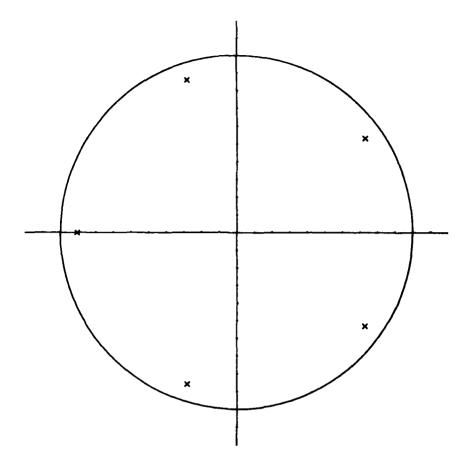
Figure 4.5.   Pole locations for an $N = 5$ stage circular shift register.

5. CHARGE DOMAIN RECURSIVE STRUCTURES

A structure which implements the real pole function is shown schematically in Figure 5.1. The impulse or unit sample response should be a decaying exponential. The charge packet representing a unit sample, X, is clocked into Section A. The equilibration gate opens and closes leaving B with $a_1 X$ and A with $k_1 X$, where

$$a_1 = C_B/(C_1 + C_B) \tag{5.1}$$

and

$$k_1 = 1 - a_1 = C_1/(C_1 + C_B). \tag{5.2}$$

The portion under A is clocked out and no new charge enters (for a unit pulse input). The equilibration gate opens and closes again storing $a_1^2 X$ in B and outputting $a_1 k_1 X$. This procedure continues giving the required exponential decay of

$$y(n) = k_1 a_1^n X \tag{5.3}$$

where $y(n)$ is the output sample and n is the sample number.

A charge domain structure called a circular shift register was developed prior to this contract to realize the transfer function of Equation 4.6.[4] This structure is shown schematically in Figure 5.2. Since it is to be a member of a family of devices in which signal samples are uniformly represented as the difference between two charge packets, it is shown with two input structures. This is a key feature which is missing from similar approaches developed by others.[9] In the figure, the positive weight charge packets enter at the top from the left, and the negative weight charge packets enter from the left

Figure 5.1   Recursive accumulator structure for implementing a real axis pole
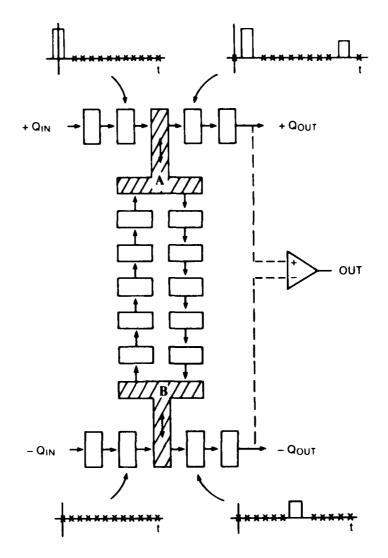
Figure 5.2. Circular shift register schematic showing impulse response.

at the bottom. Similarly, the positive weight output packets leave at the top toward the right, and the negative weight packets leave toward the right at the bottom.

Four quadrant operation (i.e., both positive and negative inputs and coefficients) is implemented by using this differential structure and by representing a positive signal sample by a charge packet of greater than the 50% of saturation level on the positive side and a corresponding charge packet on the negative side having less than 50% amplitude, while a negative signal is represented by a positive weight charge packet having less than 50% of the full potential well and a negative weight packet of more than 50% amplitude. The final output will be formed by taking the difference between the two output packets, $Q(+) - Q(-)$, which also provides enhanced common mode rejection. The operation of the circular shift register may best be understood by looking at its impulse response, i.e., tracking the output versus time (in clock periods) for a single full-scale input pulse at the $X(+)$ input at time sample $n = 0$ and with all other inputs zero. The impulse charge packet proceeds to point A where it is divided by a barrier splitter with a portion $1 - \lambda$ proceeding into the positive output channel and the λ portion following the feedback channel. The first output pulse appears with an amplitude of $1 - \lambda$. Five cycles later the λ portion has proceeded to point B where it is again split into λ and $1 - \lambda$ portions. The output portion appears as $-\lambda(1-\lambda)$ with λ^2 traveling back up towards point A. Five cycles later
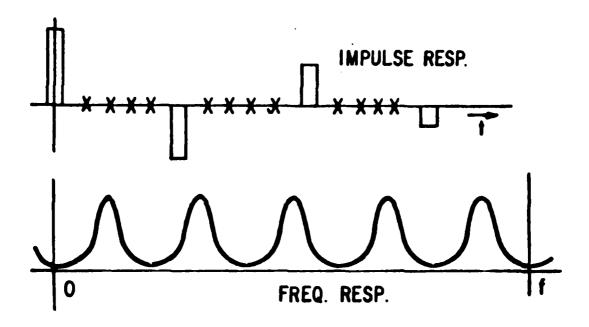
Figure 5.3.   Circular shift register impulse and frequency responses.

the split occurs at A once again with a resulting output of $\lambda^2(1-\lambda)$, and so on. This impulse response (which is the inverse Z transform of Equation 4.6) is shown in Figure 5.3. Note that any periodic signal whose period matches the time needed to complete one full circle, and which changes sign during each half period adds onto itself as it circles around the shift register. Thus, a sine wave with a period equal to the number of stages around the circular shift register builds in amplitude, and the structure also resonates at all odd multiples of this fundamental resonance. These additional harmonic resonances correspond to the additional "unwanted" poles. All other frequencies do not resonate and are attenuated. The resulting frequency response is also shown in Figure 5.3.

A charge domain transversal filter can be cascaded with the circular shift register to provide zeroes to cancel out all the higher harmonics leaving the fundamental, or cancelling out the fundamental and leaving one of the harmonics. The form of a charge domain transversal filter for leaving only the fundamental is shown in Figure 5.4. Its impulse response is a sampled data version of one half cycle of a decaying sine wave. When this impulse response is convolved with that of the circular shift register, the effect is to fill in the empty samples of Figure 5.3 with samples of the desired waveform. The impulse response of this cascaded system is the sampled data decaying sine wave shown in Figure 5.4. This truly is an infinite impulse response design. The resulting frequency response is shown in Figure 5.5. Note that now only the resonance at the fundamental frequency is apparent, all other frequencies are attenuated. This structure is capable of implementing poles essentially anywhere within the unit circle of the z-plane, with the angles expressible as

$$\theta = 2\pi n/m \tag{5.4}$$

where n and m are integers.

While this technique places poles anywhere within the unit circle, in some cases this approach, while feasible, is not practical. Suppose for instance a complex pole pair is to be placed at angle of $\theta = \pm 89°$ in the z-plane. According to Equation 4.8 this requires a circular shift register with $2N = 180$ stages. The transversal filter is required to cancel out 88 unwanted poles. In addition to being impractical in terms of size and power, the pole section, even at its non-resonance frequencies provides little attenuation, and thus the entire filter is only marginally better than the transversal filter alone.

A modification of the circular shift register concept has been discovered which provides a much more efficient way to place poles, with only a slight loss of flexibility. A standard circular shift register

5-3
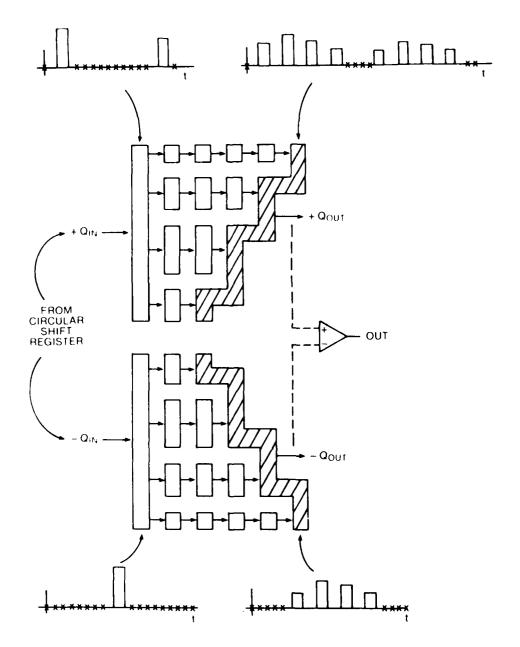
Figure 5.4. Charge domain transversal filter schematic and overall impulse response.

with $2N = 12$ stages in the feedback loop has $N = 6$ poles at angles of $\theta = (2n - 1) \cdot 30°$, $n = 1, 2, ...6$. A standard circular shift register with $2N = 14$ stages places $N = 7$ poles at angles of $\theta = (2n - 1) \cdot 25.7°$. If the circular shift register is modified to include multiple feedback loops, the poles may be placed more effectively. For instance some portion "A" may be fed back with 12 stages and some portion "B" fed back with 14 stages, where $A + B \leq 1$. By varying the A to B ratio the poles can be placed anywhere on the locus of points between the $2N = 12$ and $2N = 14$ locations as shown in Figure 5.6. Thus instead of requiring 180 stages of feedback and 88 cancellation zeroes, this technique only requires $2N = 14$ stages with 5 cancellation zeroes to place a pole at $\theta = 89°$. The only drawback is that these poles can no longer be placed arbitrarily close to the unit circle even for $A + B = 1$.

The modified circular shift register can also increase efficiency by simultaneously placing two or more sets of complex pole pairs at their desired location rather than requiring a separate circular shift register for each complex pole pair. For example the addition of a portion of $2N = 22$ and $2N = $
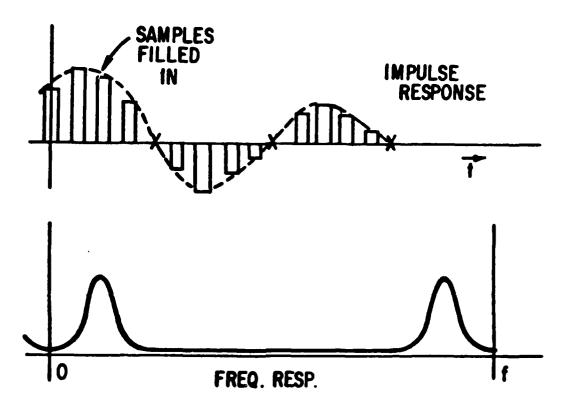
Figure 5.5. Complex pole pair impulse and frequency responses.

2 stage feedback added to a nominal $2N = 12$ stage circular shift register results in the pole-zero diagram of Figure 5.7. In this case one modified circular shift register can provide the three pole pairs of a bandpass filter centered at 1/4 of the clock, frequency. With the addition of the cancellation zeroes plus a few stopband zeroes on the unit circle a very good bandpass characteristic with a bandwidth of 1/10 of the clock frequency can be achieved with a minimal number of CCD stages. The resulting frequency response including cancellation zeroes is shown in Figure 5.8.

By combining the charge domain operations of delay, multiplication, and addition, and incorporating structures optimized for efficiency such as the circular shift register, the modified circular shift register, and the charge domain transversal filter, a wide range of filter functions can be accomplished with operating speed approaching that of a common CCD delay line. Actual filter designs which demonstrate this are described in Section 9.
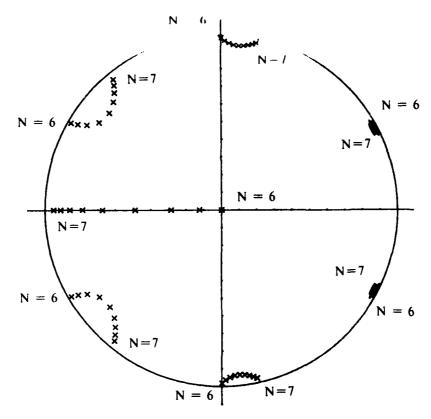
Figure 5.6. Locus of pole locations for 2N = 12 and 2N = 14 stage modified circular shift register.
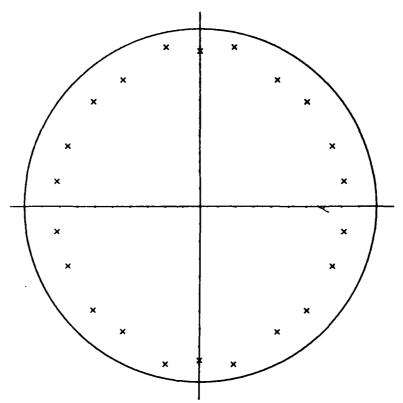
Figure 5.7. Pole-zero diagram showing grouping of poles at the imaginary axis.
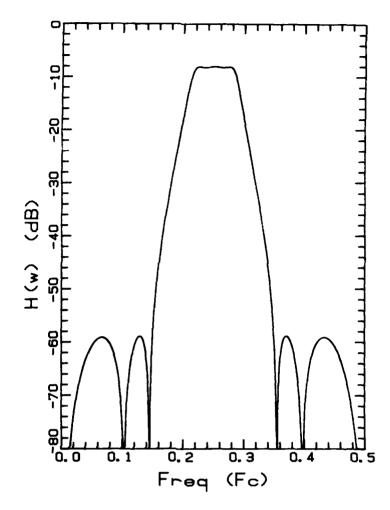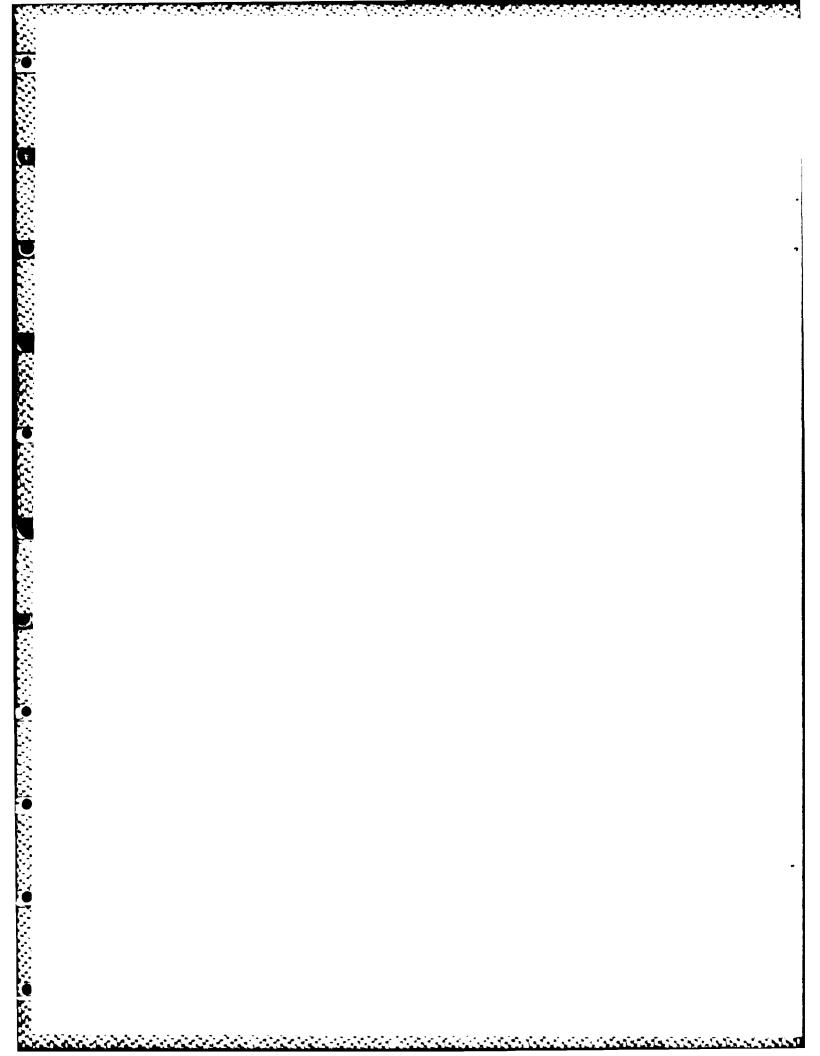
Figure 5.8.   Frequency response of a bandpass filter incorporating the pole-grouping modified circular shift register.

6. PERFORMANCE CHARACTERISTICS

6.1 LINEARITY

Since each of these functional building blocks (except for the equilibration structure) is structurally similar to a stage of a CCD delay line, each of them meets the requirements of high speed. Furthermore, since each performs its function in the charge domain with coefficients that depend only on plan-view geometry, they all provide high linearity and wide dynamic range regardless of the choice of surface or buried channel technology. The only requirement for accurate operation is efficient, unidirectional charge transfer. The speed is limited only by the onset of efficiency loss due to insufficient time for complete transfer to take place. This is a well studied problem in the context of conventional CCD delay lines, and may occur at frequencies of a few megahertz for surface channel structures with long gate lengths to several hundred megahertz for buried channel devices. Since surface channel devices utilize minority carriers and buried channel devices use "majority carriers" in a depleted region, both of which are strictly conserved in the transfer process, linearity is excellent in the summation operation for a wide variety of conditions. For example, even with buried channel technology, when two charge packets are clocked into a common output reservoir the output charge packet is equal to the sum of the two input packets regardless of their size or minor variations in threshold voltage. The noise sources that affect the dynamic range are kTC noise associated with the initial sampling process at the input and transfer noise associated with incomplete charge transfer. This latter noise source should be negligible for a high transfer efficiency CCD process. The secondary effects of the charge splitting operation, e.g., splitting accuracy, linearity, and threshold voltage effects, are discussed in Section 6.3.

6.2 DYNAMIC RANGE

The dynamic range of a charge domain system is limited by the maximum available potential well depth and the various noise sources. With the assumption that kTC noise is dominant, the signal-to-noise ratio is a function of the device size, the clocking voltage, and the sampling frequency. The maximum charge packet is

$$Q_{max} = C_{in} V_{max} \tag{6.1}$$

and the noise charge is

$$Q_{noise} = (kTC)^{1/2} \tag{6.2}$$

where V_{max} is the maximum change in potential in a CCD well before the charge spills into adjacent wells, k is Boltzmann's constant and T is absolute temperature. For a typical sized CCD the input capacitance may be

$$C_{in} = 500\mu m \times 10\mu m \times 5\times10^{-4} pF/\mu m^2 = 2.5 pF \quad . \tag{6.3}$$

Thus the input dynamic range is

$$S/N = \frac{Q_{max}}{Q_{noise}} = \frac{(2.5 \times 10^{-12})(2)}{[(1.38 \times 10^{-23})(300)(2.5 \times 10^{-12})]^{1/2}}$$

$$= 4.91 \times 10^4 = 94 dB \quad . \tag{6.4}$$

Typical values of dynamic range for charge domain devices assuming no insertion losses will be 80-100 dB depending on size. A larger device exhibits a wider dynamic range, but at the penalty of higher power consumption, lower device yield, and higher splitting errors due to threshold voltage variations depending on the threshold voltage autocorrelation distance.

Another noise sources to be taken into account is charge transfer noise

$$I_N = 2 \ln N_{ss} kT \ln 2 \tag{6.5}$$

where N_{ss} is the surface state density, A is the CCD area per stage and n is the number of transfers

Since the number of transfers is typically very small for charge domain devices, the effect of this noise source is small. The kTC noise of the output charge-to-voltage conversion circuits, typically a reset-and-float diffusion, can be taken out by correlated double sampling after amplification. The Johnson noise of the output amplifier can be calculated and can be kept small due to the small output capacitance of the CCD. The amplifier $1/f$ noise is also effectively cancelled out by the correlated double sampling operation when these devices are operated at their typical clock frequencies of > 1 MHz.

6.3 COEFFICIENT ACCURACY

Minority carrier charge-packet splitting is used in charge domain devices to implement fractional multiplication by filter coefficients. Since high precision coefficients are needed for the proper implementation of various filters, it is important to determine and accurately control the factors that influence the accuracy and noise of this operation.[10]

The concept of charge-packet splitting is to divide the charge in a CCD register into portions of the total input charge packet, where each portion is manipulated independently. A simple way for performing this operation is to divide the main CCD channel into sub-channels by inserting field oxide barriers into the channel at specific locations. The resulting charge-packets are proportional to the widths of the channels determined by the barriers.

These barriers can be constructed in several different configurations. First, the shape of the leading edge of the barrier may be designed to be either truncated (blunt) or gradual (point edge). In the case of the blunt barrier, the minority charge carriers confronting the wide edge of the barrier are subject to uncertainty on the path they have to follow. Since there is a region where the carriers have no clear choice, and small uncontrolled potential gradients can become important, this structure does not yield a high splitting accuracy. The structure with the point-edge barrier has the CCD channel pinched in by half the barrier width from each side of the channel as shown in Figure 6.1. This establishes a more symmetrical configuration than the blunt edge structure, and the region where charges can be influenced by uncontrolled effects is smaller.

The existence of transfer gates and storage gates in a two phase CCD introduces two possibilities for the location of the barriers. If the leading edge of the barrier is located under the transfer gate (Figure 6.1), the charge packet is split "on-the-fly" or dynamically, as it is being transferred from one storage gate to the next one. Since the potential of the receiving reservoir is always larger than the transfer gate region, the charge cannot "backup" to go around the barriers from one channel to the other. In this configuration the split ratio is determined only by the ratio of widths of the receiving channels which is, in turn, controlled by the position of the point edge of the barrier.

The alternate technique called static splitting places the leading edge of the barrier under the storage gate (Figure 6.2). When the charge carriers are transferred into that reservoir they are distributed uniformly across the entire area, prior to being split. When the transfer gate turns on, carriers which are located to the right of the barrier (to the right of line $B-B'$ in Figure 6.2) will be transferred to their corresponding isolated channels. The initial charge distribution, and therefore the splitting ratio is determined by the ratio of areas above and below the barrier region of Figure 6.2. Carriers initially to the left of the barrier, however, will be split dynamically and the split ratio is therefore determined by a ratio of channel widths. Thus, both width and area ratios must be controlled when utilizing the static splitting technique.

In order to obtain a completely symmetrical electric field pattern at the gate where the split takes place, a set of "dummy splitters" is used, along with the actual coefficient barrier. These splitters are placed with identical spacings across the channel, and are only a few stages long (Figure 6.3). The number of these barriers should be chosen appropriately so that the incoming charge packet is divided into equal components by the set of barriers. Only one of these components eventually becomes the split-off channel, while all others are recombined after the few stages. By creating a symmetrical structure, these dummy splitters serve to ratio all aspects of the splitters in approximate proportion to the area. They compensate non-linearities due to edge effects and equalize lateral forces applied to the charge carriers. This technique is used both for dynamic and static splitting operations.

TRANSFER GATE   STORAGE GATE

FIELD
OXIDE
BARRIER

a_1

a_2

$$\text{SPLIT RATIO} = \frac{a_1}{a_2}$$
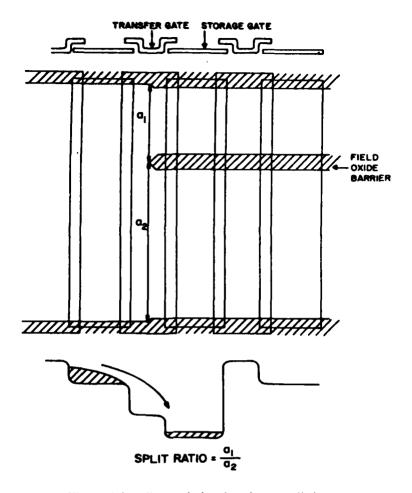
Figure 6.1.   Dynamic barrier charge splitting.

Another method of achieving charge packet splitting in CCD's is to connect the output of a CCD register to the input of two other CCD registers as shown in Figure 6.4. In this structure, the charge carriers are first equilibrated among the diodes during one clock cycle, and are transferred to the potential wells of the split-off channels on the next cycle. In this case, the capacitance ratio of the input diffusions determines the split ratio.

Experimental circuits have been designed and fabricated to investigate the packet splitting accuracies for the techniques explained above. The experiments are collected into a four-chip set which has been fabricated using double poly-silicon gate technology, 12.5 μm gate length width 7.5 μm separation.

To investigate the dependence of split accuracy on channel width and on coefficient value, split ratios designed for 0.10, 0.25, 0.50, 0.75, and 0.90 are implemented in two channel widths, 250 μm and 500 μm. The circuits realizing the 0.10 and 0.90 coefficients are also implemented with dummy splitters. For the dynamic splitting technique these experiments are organized into two chips, A and B. The designs are replicated onto chips C and D for the static splitting experiments.

The "fill and spill" method, utilizing an input diode with polysilicon gates for DC isolation, reference and signal input, is used for charge injection into the registers. The output of the CCD consists of a precharge-and-float circuit and a source follower. The same output circuit is used for the two (split) charge packets which are obtained from the same original packet, to eliminate possible output non-linearities This is accomplished by having the register with the narrow channel six cells shorter than the adjacent channel, thus providing a time delay between the outputs of the two registers
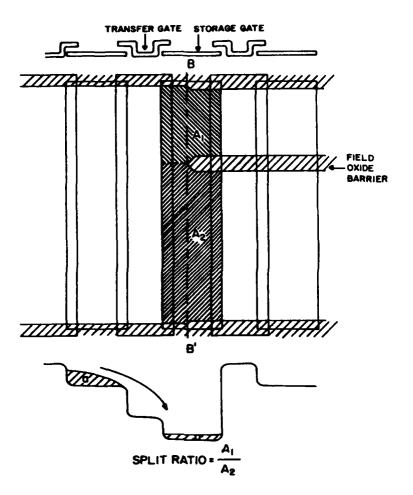
Figure 6.2. Pseudo-static barrier charge splitting.
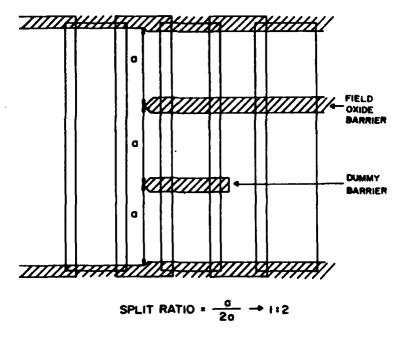
Figure 6.3. Charge splitting using dummy splitter.
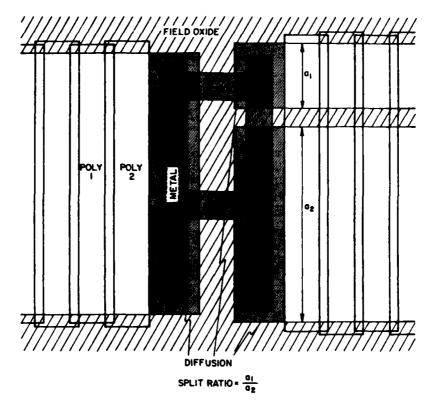
Figure 6.4. Device employing input diffusions for charge splitting.

Tables 6.5 and 6.6 list the error in the coefficients with respect to the measured geometries at 1.6 MHz, for the dynamic (ϵ_{sd}) and static (ϵ_{ss}) splitting techniques, respectively. In general it is seen that large coefficients are realized with higher accuracies than the small ones. This is due to the fact that the small coefficient error is very sensitive to the presence or absence of only a few additional charge carriers. This is particularly important in narrow channel devices, where the size of the charge packet is small. The result is that split accuracy is higher in wider channel devices, especially when small coefficients are implemented. For example, the coefficient 0.10 realized in 250 μm and 500 μm channel widths have ϵ_{sd}'s of 1.76% and 2.48% respectively, whereas the coefficient 0.90 again realized in the same dimensions have ϵ_{sd}'s of 0.29% and 0.19% respectively.

The dynamic charge splitting technique results in a higher coefficient accuracy than the static splitting, due to the fact that in the former the coefficient is determined solely by the barrier location while in the latter it is also a function of an area ratio. In the case of 0.25 and 0.75 coefficients with 500 μm channel widths and dynamic splitting, the ϵ_{sd}'s are 0.41% and 0.13%, while the 0.2459 and 0.7541 coefficients which use static splitting have ϵ_{sd}'s of 0.79% and 0.25% respectively.

The use of dummy splitters significantly increases the coefficient accuracy. For example in the case of 1:9 dynamic split, implemented with 500 μm channel, the introduction of dummies reduces the effect from 1.76% to 0.73% for the 0.10 coefficient and from 0.19% to 0.07% for the 0.90 coefficient. Blunt splitters, however, decrease the measured accuracy. Again for a 500 μm channel and a 1:3 static split, the coefficient error increases by about a factor of three when the blunt rather than sharp barrier is used. Table 6.7 lists the coefficient accuracies for dynamic splitting and 500 μm channel at 1.6 and 5.4 MHz. Comparison of these values with those at 73.5 KHz (Table 6.8) shows that errors are almost consistent up to 1.6 MHz and they slightly increase at 5.4 MHz.

The devices utilizing input diffusions for charge splitting do not provide as high accuracy as the others. Since the charge is split during the on-time of the gates next to the receiving diodes, the field oxide separating these two diffusions acts as a blunt splitter. For a 500 μm channel the 0.25 and 0.75

Table 6.5

SUMMARY OF THE RESULTS FOR DYNAMIC SPLITTING

Split Ratio	Design Channel Width (μm)	Design Coeff.	Measured Geometry	Measured Signal	ϵ_{sd}
1:1	125.0	0.50	0.5020	0.5042	0.44%
	125.0	0.50	0.4980	0.4958	0.44%
	62.5	0.25	0.2545	0.2481	2.52%
1:3 w/o D's	187.5	0.75	0.7455	0.7419	0.86%
	125.0	0.25	0.2443	0.2453	0.41%
	375.0	0.75	0.7557	0.7547	0.13%
	25.0	0.10	0.0926	0.0903	2.48%
1:9 w/o D's	225.0	0.90	0.9074	0.9100	0.29%
	50.0	0.10	0.0964	0.0947	1.76%
	450.0	0.90	0.9036	0.9053	0.19%
	25.0	0.10	0.0926	0.0938	1.30%
1:9 w.D's	225.0	0.90	0.9074	0.9062	0.13%
	50.0	0.10	0.0964	0.0957	0.73%
	450.0	0.90	0.9036	0.9042	0.07%
	62.5	0.25	0.2545	0.2255	11.59%
1:3 w/In. Diff.	187.5	0.75	0.7455	0.7745	3.89%
	125.0	0.25	0.2443	0.2401	1.72%
	374.0	0.75	0.7557	0.7599	0.56%
	25.0	0.10	0.0926	0.0665	28.19%
1:9 w/In. Diff.	225.0	0.90	0.9074	0.9335	2.88%
	50.0	0.10	0.0964	0.0802	16.80%
	450.0	0.90	0.9036	0.9198	1.79%

coefficients are realized in this case with 1.72% and 0.56% errors which are about 2 times higher than the corresponding values in the case of static splitting and a blunt barrier.

The coefficient accuracies obtained in the experiments are generally high enough to build high performance signal processing devices, and the major error sources can in some cases be compensated. Comparison of the design and physical geometries indicate that a substantial amount of error is introduced by process bias. Since physical geometries are determined by the field oxide layer, the lateral oxide growth and the isotropic etching of the nitride layer used to define the field oxide can introduce errors into the geometries. The former can be compensated by calibration of this effect and predistorting the field oxide mask. The latter can be minimized by using anisotropic etching techniques to minimize the intrinsic potential well nonuniformity at the edges of the channel. The so-called edge effect, is the second error source. The dummy splitters used to minimize this effect appear to have made a significant improvement. Frequency limitation of the drivers is the present limitation in very high frequency operation. This in turn can be substantially improved with more suitable components and RF design techniques.

Table 6.6

SUMMARY OF THE RESULTS FOR STATIC SPLITTING

Split Ratio	Design Channel Width (μm)	Design Coeff.	Measured Geometry	Measured Signal	ϵ_{sd}
1:1	125.0	0.5000	0.5020	0.4954	1.31%
	125.0	0.5000	0.4980	0.5046	1.33%
	62.5	0.2417	0.2464	0.2330	5.44%
1:3 w/o	187.5	0.7583	0.7536	0.7670	1.78%
D's	125.0	0.2459	0.2405	0.2386	0.79%
	375.0	0.7541	0.7595	0.7614	0.25%
	25.0	0.0868	0.0792	0.0710	10.35%
1:9 w/o	225.0	0.9132	0.9208	0.9290	0.89%
D's	50.0	0.09356	0.0898	0.0860	4.23%
	450.0	0.9065	0.9102	0.9140	0.42%
	25.0	0.1000	0.0927	0.0975	5.18%
1:9 w/D's	225.0	0.9000	0.9074	0.9025	0.54%
	50.0	0.1000	0.0964	0.0946	1.87%
	450.0	0.9000	0.9036	0.9054	0.20%
1:3	125.0	0.2470	0.2415	0.2469	2.24%
Blunt	375.0	0.7530	0.7585	0.7531	0.71%

Table 6.7

COEFFICIENT ERRORS VS. FREQUENCY

	Coeff.	ϵ_{sd} at 1.6 MHz	ϵ_{sd} at 5.4 MHZ
	0.10	1.76%	2.70%
Without	0.25	0.41%	0.98%
Dummies	0.75	0.13%	1.32%
	0.90	0.19%	0.29%
With	0.10	0.73%	1.87%
Dummies	0.90	0.07%	0.20%

Table 6.8

COEFFICIENT ERRORS AT 73.5 KHz

Split Ratio	Design Channel Width (μm)	Design Geometry	Measured Geometry	Measured Signal	ϵ_{sd}
1:1	125	0.50	0.5020	0.5029	0.18%
	125	0.50	0.4980	0.4971	0.18%
1:3	62.5	0.25	0.2545	0.2429	4.56%
w/o D's	187.5	0.75	0.7455	0.7571	1.56%
1:3	125	0.25	0.2443	0.2412	1.27%
w/o D's	375	0.75	0.7557	0.7588	0.41%
1:9 w/o D's	25	0.10	0.0926	0.0877	5.39%
	225	0.90	0.9074	0.9123	0.55%
1:9 w/o D's	50	0.10	0.0964	0.0933	3.22%
	450	0.90	0.9036	0.9067	0.34%
1:9 w/D's	25	0.10	0.0926	0.0919	0.86%
	225	0.90	0.9074	0.9081	0.08%
1:9 w/D's	50	0.10	0.0964	0.0970	0.62%
	450	0.90	0.9036	0.9030	0.97%

7. TESTING OF CHARGE DOMAIN DEVICES

The testing and characterization of charge domain devices can be performed either by looking at time domain or frequency domain analyses. Time domain is the chosen technique for this work and a computerized data acquisition system has been developed to analyze the results. The computer analysis program described in the next section is used to relate the time domain analysis to frequency domain results.

7.1 TESTING PHILOSOPHY

Although the ultimate goal in designing charge domain filters is to realize a certain frequency response, the devices themselves are constructed as structures which manipulate charge packet embodiments of samples of analog data in the time domain. Thus, the expected performance, and any deviations therefrom can best be understood by looking at the functioning of the charge domain building blocks in the time domain when possible. In this framework inaccuracies in the impulse response can be directly related to performance due to functions such as charge splitting errors, charge transfer inefficiency effects, or errors in the initial design. This technique has given a deeper understanding of some of the error sources in certain designs and has led to the development and demonstration of improved designs. It must always be understood however, that the final purpose is usually frequency based, and as such, the importance of time domain errors or noise must be related to frequency domain performance. This transformation can be made using computer simulation tools and is described later.

Another advantage of using the impulse or pulse response data is that averaging over many cycles of the data may be done to improve the accuracy by averaging out the noise effects. The averaging operation is used to test a wider dynamic range than may be available with a single sample through an analog-to-digital (A/D) converter. If the device noise and the A/D quantization noise are uncorrelated from sample to sample, and the signal is fully correlated, i.e., no drift terms, then the signal to noise improves with the square root of the number of readings. With this technique terms such as splitting accuracy can be measured to very high precision. Meanwhile by taking the standard deviation of these readings, the various noise sources themselves can be analyzed.

7.2 TEST STATION DESIGN

A test station has been designed and built which allowed characterization of the charge domain devices. This station consisted of two parts, the electronics to run the chip itself and a microcomputer with data acquisition capabilities to acquire and analyze the data. A block diagram for the driver electronics is shown in Figure 7.1. It consists of a voltage controlled oscillator for variable clock speeds, some TTL circuits to generate the proper timing signals, level shifters to generate the MOS clocking levels needed for the chip, and variable DC supplies for the chip. In addition there is a differential amplifier on the output and a sample and hold device. The sampled and held output is available for acquisition by the computer.

The computer includes a Z-80 central processing unit, an RS-232 terminal interface, a Basic interpreter in ROM with additional ROM for the Basic analysis programs and the operating system software. The computer also contains program RAM plus 16K of RAM storage for the data. A CRT or printer terminal can be connected for input/output. A custom A/D conversion board has been built for the system. This board allowed acquisition of the data with 12 bits of accuracy at rates up to 1 MHz. This board included the necessary timing for loading the data directly into the RAM storage. Once loaded, the data was available for analysis by the Basic analysis programs. One such program is listed in Appendix 1. This program is used to print out the time samples of an impulse or pulse response of a filter section (see Figure 7.2). The decaying sine wave impulse response can be noted starting at data point 11. Averaging of up to 100 readings (# READS parameter) can be used to improve the accuracy of these readings. The standard deviation of these readings is also printed out to give a measure of the noise on the readings and also to assure that the device noise is larger than the A/D quantization error. This tool proves to be quite valuable for measuring coefficient accuracy, system noise, and transfer efficiency. Typical measurement results are given in Section 9.

DEVICE TESTING
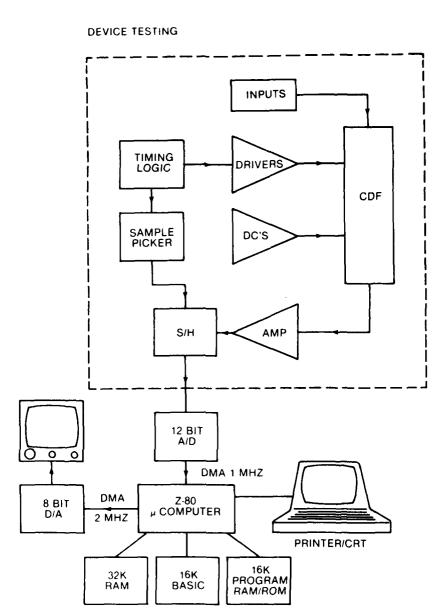
Figure 7.1. Test electronics.

Typical Output
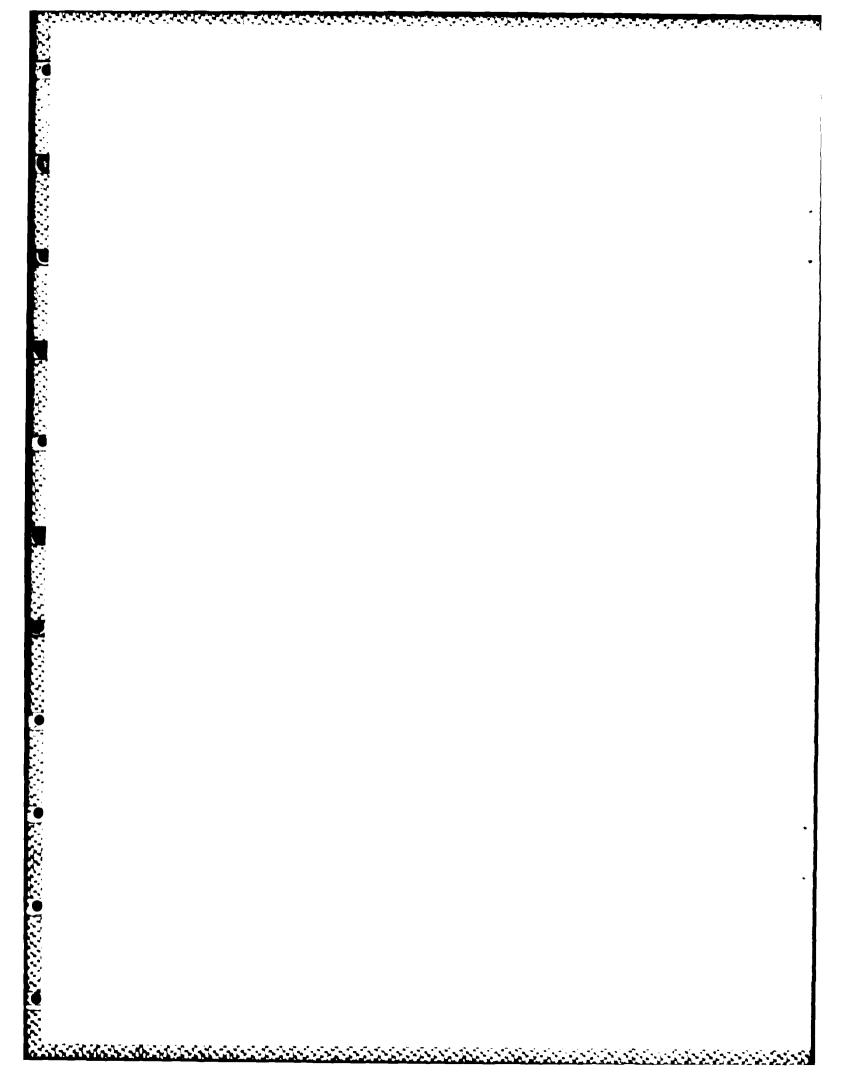
Z80-Monitor
>B

Reads, # Displayed? 4,32

Data Point #	Output Volts	Noise #Volts	Output Maxout = 1	Noise Maxout = 1
1	−6.10352E-04	1.72634E-03	−1.11545E-03	3.15497E-03
2	−3.05176E-04	1.49505E-03	−5.57725E-04	2.73228E-03
3	−1.2207E-03	3.07204E-03	−2.2809E-03	5.6143E-03
4	0	2.11432E-03	0	3.8640E-03
5	−9.15527E-04	3.62804E-03	−1.67317E-03	6.63044E-03
6	−9.15527E-04	1.79683E-03	−1.67317E-03	3.28379E-03
7	−3.05176E-24	2.49175E-03	−5.57725E-04	4.5538E-03
8	−1.2207E-03	2.90586E-03	−2.2309E-03	5.3106E-03
9	0	2.11432E-03	0	3.86403E-03
10	−3.05176E-04	2.28373E-03	−5.57725E-04	4.17363E-03
11	.115356	2.63702E-03	.21082	4.81929E-03
12	.279236	0.72958E-03	.510318	4.98844E-03
13	.426941	2.33747E-03	.780257	4.27185E-03
14	.518188	9.967E-04	.947016	1.82152E-03
15	.54718	1.22L07E-03	1	2.2309E-03
16	.515442	2.11432E-03	.941997	3.86403E-03
17	.440674	1.57592E-03	.805354	2.88008E-03
18	.338135	2.90586E-03	.617959	5.3106E-03
19	.239868	2.63702E-03	.438372	4.81929E-03
20	.146179	3.48845E-03	.26715	6.37532E-03
21	.0726318	1.9934E-03	.132738	3.64304E-03
22	.0177002	1.40955E-03	.032348	2.57602E-03
23	−.0146484	2.5411E-03	−.0267708	4.64398E-03
24	−.0292969	2.90586E-03	−.0535416	5.3106E-03
25	−.0299072	1.72634E-03	−0.D54657	3.15497E-03
26	−.0213623	3.30568E-03	−.0390407	6.0413E-03
27	−.0128174	1.72634E-03	−.0234244	3.15497E-03
28	−9.15527E-04	3.48845E-03	−1.67317E-03	6.37532E-03
29	7.01904E-03	2.28373E-03	.128277	4.17363E-03
30	.012207	2.11432E-03	.022309	3.86403E-03
31	.015564	3.34303E-03	.028444	6.19057E-03
32	.0152588	9.967E-04	.0278862	1.82152E-03

RETAKE DATA (Y OR N)? N
REPEAT CALCULATION (Y OR N)? N
OK

Figure 7.2.   Measured impulse response of charge domain low pass filter.

8. COMPUTER SIMULATIONS TOOLS

Once the time domain data is taken, it is useful to compare the experimental data with the design data. When the application involves filtering, the specifications are usually given in terms of frequency response. Therefore computer tools are required to convert the time domain data into the frequency domain so that the experimental frequency response may be determined and compared with the desired response. Computer tools are also required when undertaking the design of a new filter. The proper placement of poles and zeroes within the constraints imposed by charge domain technology can be accomplished through simulation. From these simulations it can be determined whether a filter design is practical with charge domain technology.

The computer program "DSP" has been written to address these needs. A listing is given in Appendix 2. It consists of a number of FORTRAN 66 subroutines written on a Honeywell 6000 mainframe computer. The routines cover functions used for digital (or discrete time) signal processing as well as printing and plotting routines for visualizing the outputs. The signal processing routines include routines like ZPOLR which finds the roots of a polynomial, PZIMP which calculates the impulse response from the pole-zero locations, FREQPZ which converts zero locations stated as fractions of the clocking frequency to Z-plane zero locations, PZ which calculates the frequency response from the pole and zero locations, and subroutine COEF which calculates the frequency response from the numerator and denominator coefficients of a transfer function. Other routines include FFT which performs a fast Fourier transform for converting between time and frequency domain results, MAG which converts a complex frequency response into magnitude (linear and dB) and phase information, and SAMPLE which multiplies the frequency response data by the $\sin(x)/x$ response of a data sampler. Printing routines include PRNTIMP, PRNTFREQ, and PRNTPZ for impulse response, frequency response and pole-zero information respectively, as well as PZMINMAX which prints out the local minimums and maximums of frequency response curves. The plotting routines are PLTIMP, PLTMAG, PLTPHASE, and PLTPZ for impulse response, magnitude and phase and pole-zero plots. The subroutine PLT is the general purpose X-Y plotting routine called by PLTIMP, PLTMAG, and PLTPHASE. These routines call subroutines of Hewlett-Packard's PLOT21 plotting package which interfaces with HP's 7221A pen plotter.

With the availability of these routines, a simple program, such as the one listed in Appendix 3 and excerpted in Figure 8.1, is all that is required to design a charge domain filter. The listed program was used to design the 8 pole bandpass filter which has been designed under this contract. There is one section for each of the four pairs of complex conjugate poles, and one section for the cancellation zeroes. Each section may be analyzed by itself or in combination with any or all of the various other sections. For each of the pole sections the polynomial coefficients must be specified. These correspond directly to the splitting coefficients where the polynomial subscript (actually the exponent of Z^{-1}) corresponds to the number of stages in the feedback loop. For the bandpass filter design described in Section 9, the $\theta = 91°$ poles use a charge domain stage which implements the function

$$H(Z) = .1/(1 + .6Z^{-14} + .3Z^{-17}) \tag{5.1}$$

The required polynomial coefficients for the program are PCOEF(1) = 1, PCOEF(15) = .6, and PCOEF(18) = .3. The corresponding charge domain stage has a feedback portion = .6 with $N = 14$ CCD stages of delay, another feedback portion = .3 with $N = 17$ stages, and the remaining portion = .1 sent directly to the stage output. The DSP program produces pole-zero, frequency response, and time domain plots, as well as printouts of pole and zero locations and filter coefficients. Examples of these plots and printouts are displayed throughout Section 9. The feedback coefficients and the number of stages in the feedback loop may be varied and the effect on the response can be visualized in the pole-zero and frequency response plots. Thus, each of the pole sections can be optimized under the charge domain constraints.

Once the remaining poles have been placed to shape the passband, the cancellation zeroes can be placed to cancel out the spurious poles. This is done by placing the transversal filter zeroes on the unit circle at the frequencies of the spurious poles. This is demonstrated in the listing of Figure 8.1 where the zero locations are specified as positions on the unit circle as a fraction of the distance around the unit circle (i.e. as a fraction of the clocking frequency). Finally, the overall frequency response and pole-zero plots of the filter design can be displayed and compared with the filter specifications.

```
C***********************************************
C
10      print *, ` `
        print *, '91 DEG POLES'
        NPOLE=17
        DO 12 I=1,NPOLE+1
12      PCOEF(I)=0.
        PCOEF(1)=1.
        PCOEF(15)=.6
        PCOEF(18)=.3
        KLAB=30
        CALL CALCPOLE
        DO 14 I=1,N
14      G(I)=G(I)*H(I)
C
C***********************************************




C***********************************************
C 40    print *,` `
        print *,'ZEROS'
        NPOLE=0
        NFREQ=6
        DATA (ZFREQ(I),I=1,6) /.0325,.108,.180,.320,.392,.4675/
        KLAB=20
        CALL CAL CZERO
        DO 46 I=1,N
46      G(I)=G(I)*H(I)
C
C***********************************************
```

Figure 8.1.   Partial listing of bandpass filter design program.

This program has been invaluable in the development of design methodologies for charge domain devices, and in analysis of their experimental performance. The program has recently been upgraded to FORTRAN 77 on a Digital Equipment Corporation VAX 11/782 computer. The plotting routines have also been enhanced with such features as windowing and curve smoothing and allow plotting on Tektronix graphics terminals as well as Hewlett-Packard pen plotters. Thus, quick visual feedback is available on a CRT terminal, with hard copy plotting once the design has been confirmed.

9. CHARGE DOMAIN FILTER EXPERIMENTAL RESULTS

The second goal of the contract as listed in Section 1, was the design and fabrication of a test vehicle filter which demonstrates the unique capabilities of the charge domain approach. Before embarking on the design of a test vehicle filter, an analysis of an existing charge domain lowpass filter chip "CDF1" was undertaken. These results led to a decision that a redesign of the low pass charge domain filter would provide further insight into design considerations. This redesigned chip entitled CDF2, exhibited much improved performance over our earlier design. Following this accomplishment, the design of a high performance bandpass filter was attempted. This exercise led to a thorough understanding of the design tradeoffs which optimize charge domain filter designs. An 8-pole narrowband filter was chosen as the test vehicle, because its simulated performance was unachievable with alternative technologies. The design was implemented in silicon and the resulting chips entitled CDF4 demonstrated a frequency response which matched the simulations very closely.

9.1 CHARGE DOMAIN LOW PASS FILTER

9.1.1 First results — CDF1

The design concepts described in Section 2 have been utilized in the design of the first three pole charge domain filter "CDF1." A Butterworth low pass filter has been chosen for simplicity of design while still demonstrating the charge domain concepts of charge splitting, equilibration, feedback and cascading of sections. The design requires a recursive accumulator to implement the real axis pole and the complex pole pair is implemented by a circular shift register in combination with a cascaded transversal filter to provide the cancellation zeroes. The chip has been layed out and fabricated in the GE processing facility in Schenectady, NY.

A photomicrograph of the chip is shown in Figure 9.1. The chip contains two fill-and-spill input sections (positive and negative inputs), two recursive accumulators to implement the real pole, a 16-stage recursive loop to provide the 8 poles around the unit circle, two 7-stage transversal filters to cancel out 6 of those 8 poles, and two output sections (positive and negative output). The device has been processed in 7.5 μm p-channel technology (12.5 μm long storage gates with 7.5 μm long transfer gates). The chip size is 55 × 88 mil² including the large area used for bonding pads. Chip power is less than 10 mW at a 1 MHz clock frequency. A pseudo-one phase clocking scheme is used to move the charge packets and 10 μ wide thick oxide barriers (narrowed to a point) are used to split the charge packets.

A number of test devices are included in the mask set so that each of the subsections of the filter can be tested individually. The time response of several of these subsections is shown in Figure 9.2. Figure 9.2a shows the impulse response of the transversal filter alone. This is a finite impulse response filter with 7 non-zero values as can be seen from the Figure. When the circular shift register is included, the response continues as a decaying sine wave for an infinite number of cycles as shown in Figure 9.2b and 9.2c. The impulse response of the real pole section of Figure 9.2d is seen to be the expected decaying exponential. The impulse response of the entire filter is shown in Figure 9.2e.

These time domain responses have been analyzed in detail by the computer data acquisition system described in Section 7 and the simulation tools described in Section 8. This analysis enables a number of design problems to be isolated. While the device demonstrates the feasibility of the charge domain approach, these problems limits its performance in several ways.

A design error causes the feedback coefficient for the recursive loop to be too small, thus giving incomplete cancellation of the excess poles by the zeroes. Even when this error is taken into account, the measured feedback coefficient is in error and showed poor linearity. This problem is caused by the equilibration splitting technique itself. Whenever equilibration splitting is to be used (either gated or non-gated) great care must be taken to properly ratio all significant splitting parameters, namely storage area oxide capacitances, storage area diffusion capacitances, channel widths, and gate area itself. This topic is be described in more detail in the section on filter redesign.

The charge domain transversal filter has been analyzed in great detail, and the results are listed in Table 9.3. Errors in the actual response are on the order of 1% when compared to the design values. However when the geometrically measured coefficients are compared to the electrically measured
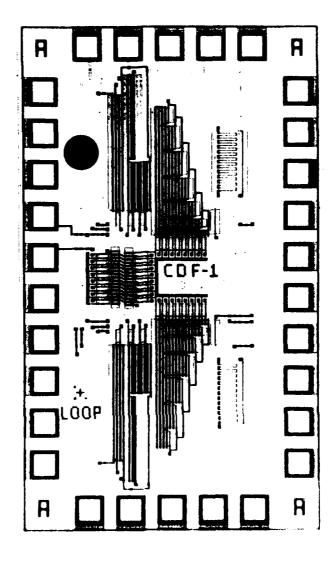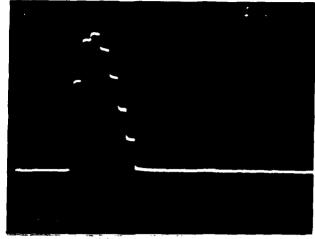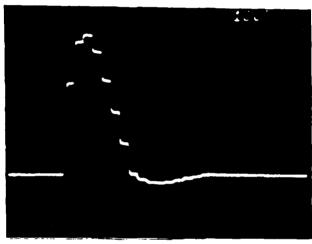
Figure 9.1.   CDF1 photo micrograph.

coefficients, the agreement is much closer. The discrepancy between the designed and the actual channel widths is due to geometry alterations which occur during device processing. This error has been reduced in subsequent devices by predistorting the mask design to compensate for this effect. With this compensation and other improvements described in Section 6.3, the dynamic charge splitting technique provides a very accurate and linear means for determining coefficients.

The configuration of the real pole (Figure 9.4) section causes a number of problems. In this approach a charge packet enters storage area A. The equilibration gate is turned on causing the surface potential of storage areas A and B to equilibrate. When the gate is turned off the charge should be split in the same ratio as the areas. Unfortunately the charge under the equilibration gate does not split by the proper ratio as the gate is turned off but usually splits closer to a 1:1 ratio because of the charge under the gate region itself, which tends to split equally as the gate is turned off. This effect causes a 3% error in the coefficient of the real axis pole. A solution for this problem is described in the next section.

(a) Transversal filter
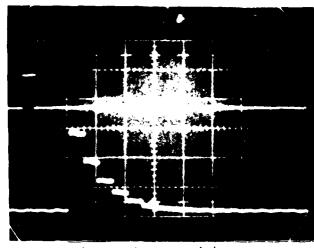
(b) Circular shift register
plus transversal filter
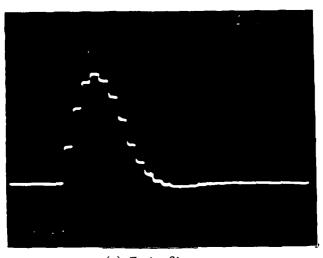
(c) Figure 9.2b at high gain

Figure 9.2. CDF1 impulse Response

(d) Recursive accumulation

(e) Entire filter

Figure 9.2.   (Cont'd)

Another problem with the configuration of Figure 9.4 is the long gates of the output section C. For saturation charge handling capabilities the area under electrode C must equal the area under electrode A, and since the width is confined the length is increased from 12.5 to 30 μm. The transfer inefficiency of these long stages causes the clocking speed of these devices to be limited to less than 1 MHz (Figure 9.5). This problem has also been overcome in the redesign. It is noted that the lateral equilibration using metallized diffusions was very fast and does not provide any speed limitation for these devices.
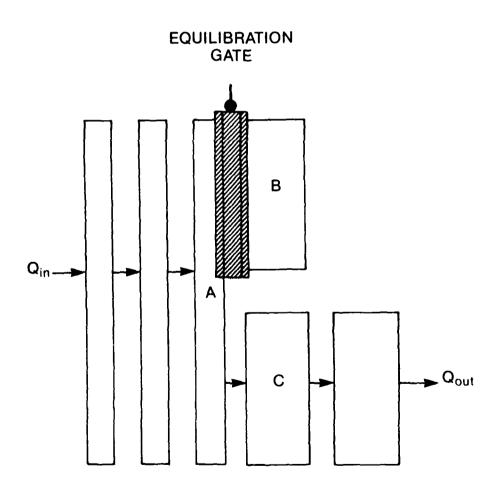
Finally it is noted that harmonic distortion is quite low −55 to −60 dB due to using differential (positive and negative) signal processing (Table 9.6).

9.1.2 The Redesign − CDF2
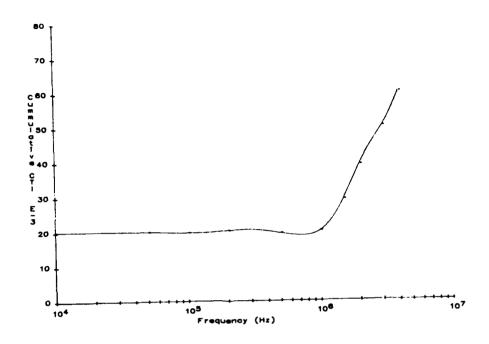
A redesign of CDF1 has been completed in order to optimize the performance of the low pass filter, and to overcome the faults which are apparent in the operation of CDF1. The three pole Butterworth filter characteristic is improved by moving the poles to the following locations:

Table 9.3

CDF1 CHARGE SPLITTING ACCURACY RESULTS

Coefficient	Design	Geomtry	Experiment
1	.1396	.1379	.1382
2	.2013	.2018	.2002
3	.2078	.2082	.2079
4	.1818	.1814	.1818
5	.1364	.1367	.1373
6	.0877	.0894	.0905
7	.0455	.0447	.0441

EQUILIBRATION
GATE

Q_{in} →

B

A

C

Q_{out}

Figure 9-4   CDF1 real pole section
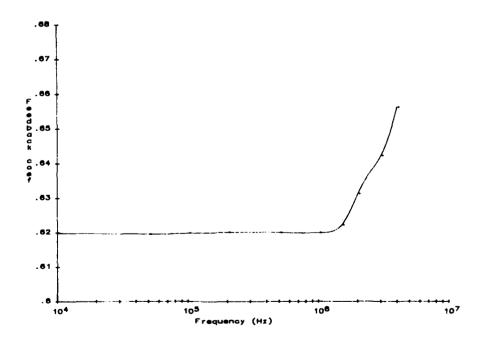
Figure 9.5. Charge transfer inefficiency and its effect on the recursive accumulator.

Table 9.6

**HARMONIC DISTRIBUTION FOR A CLOCK FREQUENCY OF 100 kHz
AND A SIGNAL FREQUENCY OF 1 kHz**

F Out (kHz)	V Out (mV)	V Out (mV)	V Out (mV)	V Out (mV)	V Out (mV)
1	10	100	300	1000	3000
2	.0045	.004	.15	.32	7.8
3	.0040	.015	.005	.17	950
4	.0035	.008	.06	.08	3.0
5	.0030	.008	.005	.06	5.1

(Note: all voltages are rms values)

$P_1 = 0.714$
$P_2 = 0.778 + j\,0.332$
$P_3 = 0.778 - j\,0.332$

This provides an equi-ripple type frequency response with less passband attenuation, greater stopband attenuation and a sharper transition region (Figure 9.7).
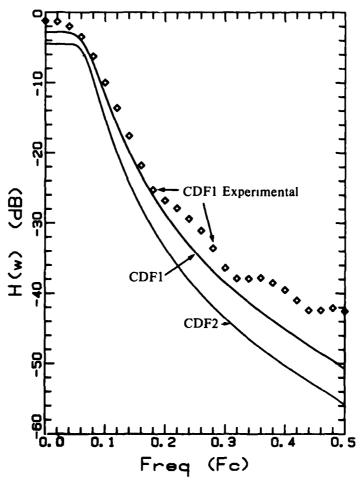
Figure 9.7.   Comparison of the frequency response of CDF1 and CDF2.

An attempt has been made to overcome each of the deficiencies of the previous filter with the main goals being improved accuracy and speed performance. This device has been produced with n-channel technology and with design rules shrunk by 20%. This yielded a 10 μm storage gate length and 6 μm transfer gate length. The saturation charge capability is therefore reduced and the low frequency transfer inefficiency increases, but the maximum clocking speed should be increased. The pseudo-one phase clocking scheme is maintained and the thick oxide barrier width is shrunk to 8 μm. A number of design changes have been incorporated and the improvements have been successful. The finished chip photomicrograph is shown in Figure 9.8.

This time dynamic splitting with barriers is used to determine the feedback coefficient for the recursive loop, rather than the equilibration scheme used for CDF1. This leads to much improved coefficient accuracy and linearity. The old "form − C" structure and new "Figure − 8" structure approaches are compared in Figure 9.9. Mask predistortion is used and coefficient accuracy for the feedback coefficient (0.05% error) and the transversal filter coefficients (0.1 − 0.2%) is much improved (see Table 9.10).

Two different techniques of overcoming the deficiencies of the real pole section (shown again in Figure 9.11a) have been evaluated. The first one is once again a gated equilibration technique. Here, however, the incoming charge packet is dumped into the storage area B rather than A (see

CHARGE DOMAIN FILTERS — CDF2

Figure 9.8.   CDF2 photomicrograph.
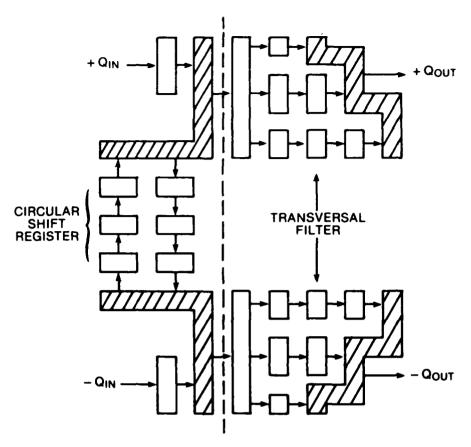
Figure 9.9a. "Form − C" structure for implementing complex pole pairs.
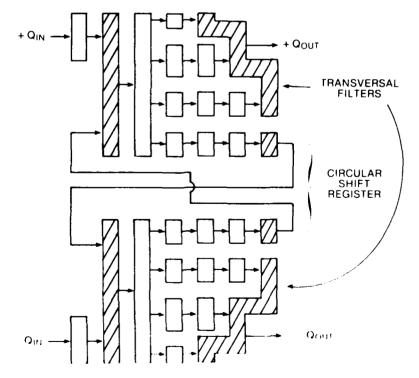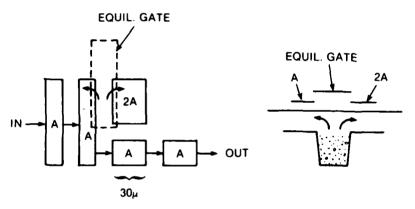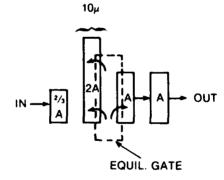
Figure 9.9b. Figure − S structure for implementing complex pole pairs.

Table 9.10

CDF2 TRANSVERSAL FILTER COEFFICIENT ACCURACY
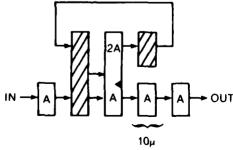
Coef.	Theory	Actual Size	100 KHz Exp.	29 MHz Exp.
1	.585	.572	.565	.555
2	.909	.906	.915	.909
3	1.000	1.000	1.000	1.000
4	.911	.910	.916	.909
5	.709	.704	.705	.721
6	.456	.451	.458	.472
7	.208	.202	.206	.221
FB	1.204	1.207	1.200	1.209

(a) Equilibration technique used for CDF1

(b) Equilibration technique used for CDF2

(c) Barrier charge splitting technique used for CDF2

Figure 9.11. Recursive accumulator structures.

Figure 9.11b). This necessitates a wider structure to accomodate the saturation signal, but it does not incorporate any long gates and thus is much faster than the earlier approach. In addition great care has been taken to properly ratio all capacitances and to properly ratio the amount of stored charge under the equilibration gate as it is turned off. The resulting device shows high accuracy (0.2% error) and operates at high speed (to > 10 MHz).

The second approach is an attempt to use dynamic (barrier) splitting to determine the coefficient. A barrier split with a single stage feedback loop is implemented as shown in Figure 9.11c. Here, however, lateral equilibration in front of sectionA and 2A is not instantaneous and much of the charge coming out of the feedback loop, 2A, stays at the 2A end and does not divide properly. Accuracy is good (1% error) but degrades with frequency and signal level. A design improvement is described later which improves the accuracy and speed of this approach to levels similar to or better than the gated equilibration technique.

The speed limitations of the device are caused once again by transfer inefficiency. Transfer inefficiency has been measured on 128 stage CCD test devices. Results are shown in Figure 9.12 for both the 7.5 μm device and a 6.0 μm device. The 6 μm device has higher inefficiency at low frequency since the width is also scaled down from 125 μm to 100 μm. The speed improvement is slight and indicates that further shrinkage and/or buried channel processing are required to attain the full potential of the charge domain concept.

Due to the small number of stages required for CDF2 the coefficient accuracy holds up reasonably well out to near 20 MHz. The test box has been modified to run up to 35 MHz and the devices are still functional although the accuracy degrades due to transfer inefficiency.

Besides speed and accuracy, the dynamic range is improved. Total dynamic range at 1 MHz clock rate measures 86 dB saturation signal to RMS noise. In the linear range of operation, 80 dB is routinely achieved.

9.2 BAND PASS FILTER

Following the successful redesign of the low pass filter, a search has been made to find a filter function which can not conveniently be constructed with conventional technologies and pushes the limits of

Figure 9.12 Charge transfer inefficiency vs. frequency for 6.0 micron and 7.5 micron processes.

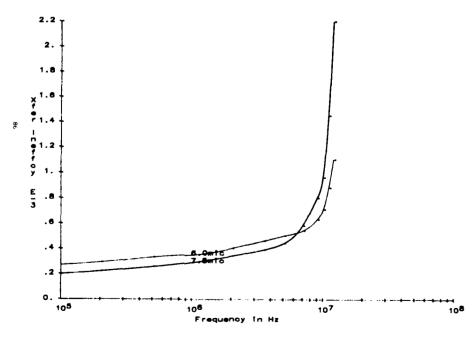charge domain technology. This test vehicle filter has been designed, built and tested to indicate the ultimate potential for CDF's in high performance systems.

9.2.1 Filter Design Considerations

Both narrow- and wide-band multi-pole bandpass filters have been investigated as potential test vehicle filters. The wide band filter appears to be a natural candidate for the charge domain approach, since a single modified circular shift register can provide six of the desired poles simultaneously. The frequency response of such a filter is discussed in Section 4.

While this approach yields an excellent filter with a very efficient design, it does not address the generic case of filter design. A narrowband filter design, if it can be done in the charge domain, is a better challenge to test the limits of CDF capabilities. The task which has been attempted is the design of a multi-pole bandpass filter with a bandwidth of 1/100 of the clock frequency (Fc). In addition the passband itself should be flat and the skirts should be very steep (down >16 dB at 2/100 Fc bandwidth) to simulate the requirements of a realistic FM communications system. The sidelobes should be attenuated more than the 40-45 dB typically achieved with conventional CCD split electrode filters and the output dynamic range should be kept as large as possible, say 60 dB or better. These constraints turn out to be quite difficult to meet with the concepts discussed thus far due to some of the design considerations discussed below.

The main advantage of using CDF's is that all processing internal to the filter is performed with charge packet manipulation. This allows filter sections to be easily cascaded to build up complex filter functions with no overall loss in clocking speed. The drawback to this approach is that because there are no gain elements in the structure, each of the sections can only attenuate the signal. Thus if a number of stages are cascaded the attenuation in the passband (insertion loss) may become quite large. Since the dynamic range of these devices is limited to about 80 dB at the input, this insertion loss can severely degrade the filter's performance.

These constraints have led to a design methodology which should be followed with these devices. The underlying philosophy is that

> when sections are to be cascaded, the passband of
> all sections should be as similar as possible and
> should be designed for minimum insertion loss in
> the pass band. This will optimize the overall dynamic
> range.

The advantage of this philosophy is demonstrated in Figure 9.13 which shows two approaches for implementing a bandpass filter. The first is a conventional cascade of single pole sections. In this case the A pole attenuates in the B pole's passband and vice versa. Thus the overall passband has a large insertion loss. The second approach uses two sections such as a modified circular shift register cascaded with a charge domain transversal filter, where the two sections have overlapping passbands. The same overall passband shape may be achieved with much less insertion loss, thus significantly improving the overall dynamic range.

A second major advantage of the modified circular shift register can be appreciated in the context of this design philosophy, for it sometimes permits more than one of its pole pairs to be used, thereby eliminating the need to cascade two conflicting frequency responses. This is accomplished by starting with a circular shift register with poles close to all of the desired locations, and then moving these around by adding additional resonant channels so that the pole locations simultaneously move to the desired places. The charge domain transversal filter is an ideal vehicle for providing many zeroes at once, and the modified circular shift register discussed above can be used for implementing several poles at once. These more general types of sections have enough flexibility to provide the desired frequency response, while greatly reducing the insertion loss as well as chip size and power compared to a cascade of simple sections.
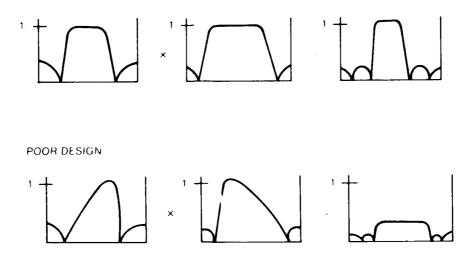
GOOD DESIGN

POOR DESIGN

Figure 9.13. Minimizing insertion loss in charge domain filters.

9.2.2 The Filter Design — CDF3

The choice of the narrowband bandpass filter, however, pushes beyond the limits of this approach and leads to an extension of it, namely the idea of using a partial fraction expansion as an alternative to a cascade.[11] In order to make a narrowband filter with a flat passband the poles must be closely spaced. The center frequency is chosen to be at 1/4 of the clock frequency which leads to clustering of the poles around the imaginary axis (or $\theta = 90°$ line) of the z-plane. This choice yields the most space-efficient designs while providing maximum separation of the alias band responses. According to the equation

$$\theta = (2^{n-1})360/2N \quad n = 1,2,\cdots N \tag{9.1}$$

feedback loops with $N = 2, 6, 10, 14, 18 \ldots$ stages of feedback result in poles located at $\theta = 90°$. A great deal of time has been spent trying to modify a circular shift register to provide a close cluster of poles around the imaginary axis. While this approach works quite well for the wideband filter, the narrowband design calls for too many stages in the feedback loop to be practical. At this point the fallback position is again to implement each pair of poles by itself and cascade the sections.

For a bandpass filter centered at $\theta = 90°$ and with a bandwidth of about $360°/100 = 3.6°$ pole pairs should be located at approximately 89°, 90°, and 91°. The next step is to choose the amount of feedback and the number of stages of feedback required for each of the sections. The equation

$$|Z| = (-\alpha)^{1/(2N)} \tag{9.2}$$

implies that increasing the feedback portion, α, towards its maximum value of 1 and increasing the number of stages, N, will give poles closer to the unit circle. However, increasing the feedback portion or increasing the number of stages of feedback leads to a larger chip size with higher power consumption. Decreasing the Q on the poles reduces the flatness of the passband and the steepness of the skirts.

In order to choose a "good" design a feedback limit of 90% has been chosen. The number of stages in the feedback loop becomes the parameter that can be varied to meet the performance goals. The 90° poles can easily be implemented with $N = 2$, so the design of the 89 and 91° poles are undertaken first. A modified circular shift register structure as described in Section 2 is used with the majority of the feedback portion on $N = 4n - 2$ stages where $n = 1, 2, \ldots$ with a smaller portion on the $N = 4m - 2 + 1$ state, where $m = 1, 2, \ldots$ and is not necessarily equal to n. The total feedback

portion is 90°. The value of n is the minimum which satisfies the Q requirements on the pole. The possibilities for m = n = 2, 3, 4, and 5 are plotted in Figure 9.14 with the ratio of $\Delta n = 2$ to $\Delta n = 1$ feedback varied from zero to one for each case. A value of $n = 4$ which requires $N = 14$ has been chosen for both the 89° 91° poles. The ratio of $N = 14$ to $N = 13$ feedback is chosen to place the pole at the desired 91.9° angle. When this same ratio is applied for the 89° pole, i.e., the $N = 14$ to $N = 15$ ratio, the pole responses are not symmetric around 90°. Further fine tuning leads to the following feedback values:

	N	α_n
91° poles:	14	.6
	17	.3
89° poles:	14	.6
	15	.1
	19	.2

The resulting frequency response for both of these filter sections is shown in Figure 9.15 with an expanded view of the area of interest shown in Figure 9.16.

When these two sections are cascaded the resulting frequency response is as shown in Figure 9.17. As discussed earlier the cascading operation leads to a undesirably large insertion loss, so some way
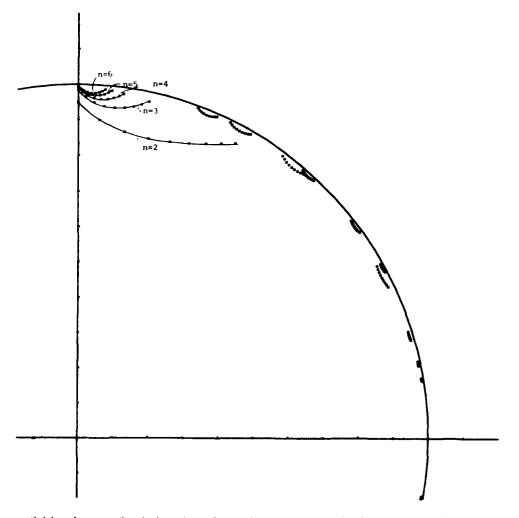
Figure 9.14 Locus of pole locations for various number (n) of stages in feedback loop.

9-14
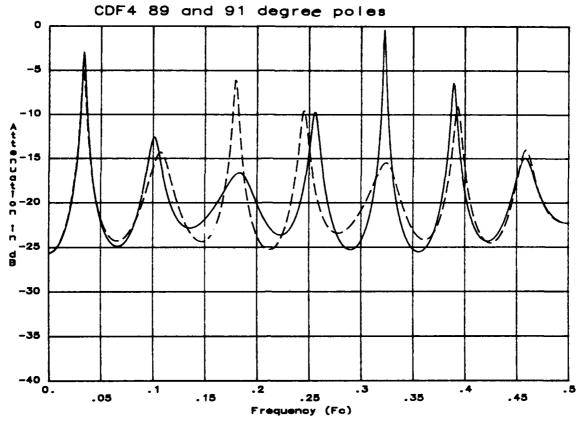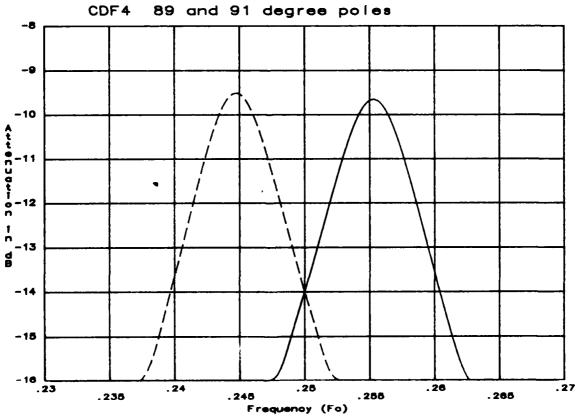
CDF4 89 and 91 degree poles

Figure 9.15. Frequency response for 89° pole section (dashed) and 91° pole section (solid).

CDF4 89 and 91 degree poles

Figure 9.16 Frequency response for 89° and 91° pole sections near center frequency.

CDF4 parallel vs. cascade
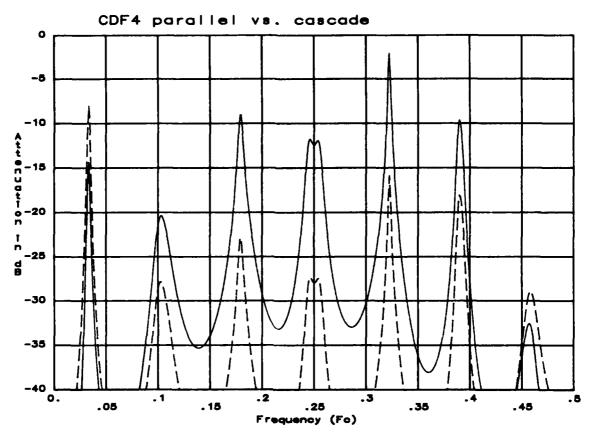
Figure 9.17. Frequency response for cascade (dashed) and parallel (solid) connection of the 89° and 91° pole sections.

must be found to implement the resonances of both modified circular shift registers in a single structure. Although there are several possibilities for doing this, a relatively simple solution has been found that proved satisfactory, namely a parallel architecture which is equivalent to a partial fraction expansion of the transfer function. The resulting response, which is compared to the cascade response in Figure 9.17, reduces the designed-in insertion loss by 13 dB, which is enough to make this design practical.

Two 90° pole pair sections are added in order to flatten the passband and provide sideband attenuation. The resulting parameters for these sections are $N = 2$ stages and $\alpha = .875$ feedback. These sections can be combined in cascade with the 89° and 91° parallel combination since, as seen in Figure 9.19, the passbands overlap in the area of interest.

Finally the transversal filter section is added. The zeroes of this filter are placed on the unit circle (see Figure 9.20) to cancel the undesired poles of both of the other sections. Also, by placing the zeroes symmetrically around the $\theta = 90°$ line, every other coefficient of the transversal filter becomes zero. The frequency responses of this section (see Figure 9.21) also has a passband which overlaps that of the other sections and can therefore be cascaded with little additional insertion loss.

The resulting pole and zero locations are shown in Figure 9.22 and are listed in Table 9.23 with the overall frequency response shown in Figure 9.24. Figure 9.25 gives an expanded view of the passband. The original design goals have been met and the resulting filter, if it can be fabricated, promises impressive performance. The passband is flat to 1 dB over 1/120 Fc, the 3 dB bandwidth is 1/100 Fc, the response drops off by 18 dB at 2/100 Fc, and by 60 dB at 5/100 Fc. The overall insertion loss is only 12 dB so that with an input dynamic range of 80 dB, the output stopband noise floor is −68 dB with respect to the passband.

It can be seen from this design exercise that the computer design tools are invaluable, not only in design optimization, but in the development of the design methodology.

CDF4   90 degree poles
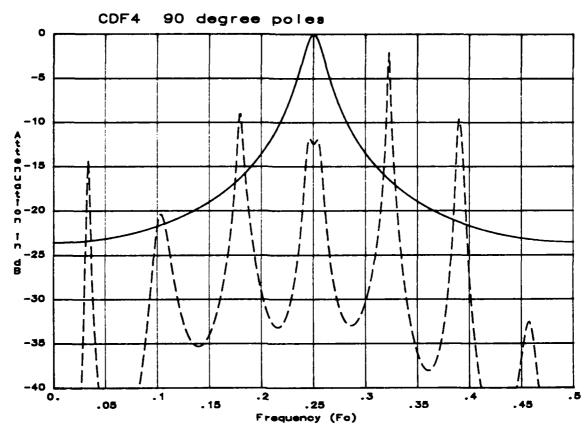
Figure 9.19.   Frequency resonse for 89°-91° pole sections (dashed) and 2 90° pole sections solid.
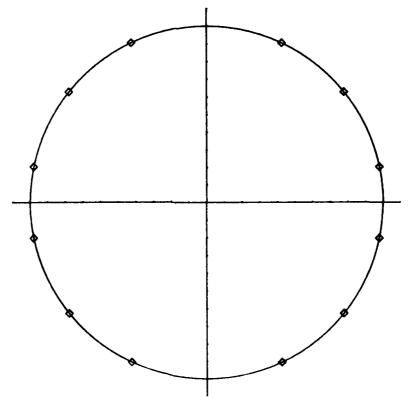
Figure 9.20.   Zero locations (diamonds) for transversal filter section.

CDF 4 cancellation zeroes
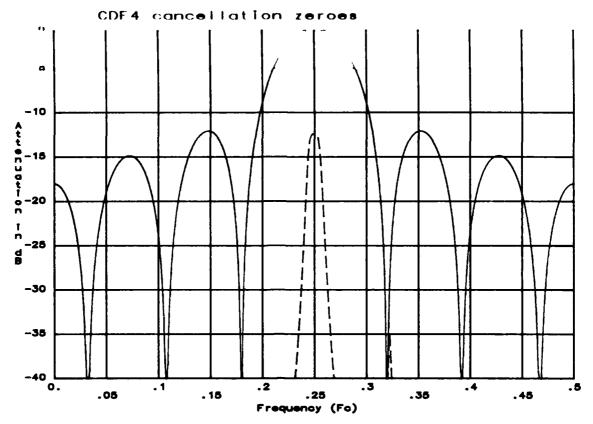
Figure 9.21. Frequency response of 89-91-90-90° pole sections (dashed) and of zero section (solid).
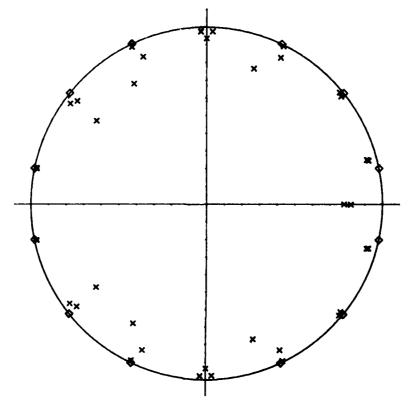
Figure 9.22. Z-plane pole-zero plot for charge domain bandpass filter.

Table 9.23

POLE AND ZERO LOCATIONS FOR THE BANDPASS FILTER DESIGN

run cdf4
Output file name: cdf4

91 DEG POLES
do you want to include this? y

POLE LOCATIONS

#	REAL	IMAG	RADIUS	ANGLE	FREQ (FC)
1	−0.4352	0.8922	0.9927	116.0035	0.3222
3	0.9684	0.2058	0.9900	11.9956	0.0333
6	0.3621	0.8328	0.9081	55.5990	0.1847
7	−0.9086	0.2511	0.9427	164.5505	0.4571
9	−0.7544	0.6327	0.9846	140.0152	0.3889
11	0.7766	0.5688	0.9626	36.2207	0.1006
13	−0.0328	0.9752	0.9758	91.9235	0.2553
15	0.4141	0.5807	0.7968	58.6873	0.1630
17	−0.7804	0.0000	0.7804	0.0000	0.0000
18	0.0000	0.0000	0.0000	90.0000	0.2500

Do you want to plot this?

89 DEG POLES
Do you want to include this? y

POLE LOCATIONS

#	REAL	IMAG	RADIUS	ANGLE	FREQ (FC)
1	0.4245	0.8894	0.9855	64.4847	0.1791
3	−0.9205	0.2492	0.9537	164.8539	0.4579
5	0.0327	0.9761	0.9766	88.0830	0.2447
7	0.9661	0.2026	0.9871	11.8447	0.0329
9	−0.7642	0.6110	0.9785	141.3573	0.3927
11	−0.4212	0.8293	0.9301	116.9281	0.3248
13	0.6255	0.4733	0.7844	37.1122	0.1031
15	−0.2680	0.7675	0.8129	109.2451	0.3035
17	0.7351	0.5848	0.9393	38.5023	0.1070
19	−0.8198	0.0000	0.8198	0.0000	0.0000
20	0.0000	0.0000	0.0000	90.0000	0.2500

Do you want to plot this?

90 DEG POLES
Do you want to include this? y

POLE LOCATIONS

#	REAL	IMAG	RADIUS	ANGLE	FREQ (FC)
1	0.0000	0.9354	0.9354	90.0000	0.2500
2	0.0000	−0.9354	0.9354	−90.0000	−0.2500

Do you want to plot this?

90 DEG POLES

Table 9.23 (Cont'd)

POLE AND ZERO LOCATIONS FOR THE BANDPASS FILTER DESIGN

Do you want to include this? y

POLE LOCATIONS

#	REAL	IMAG	RADIUS	ANGLE	FREQ (FC)
1	0.0000	0.9354	0.9354	90.000	0.2500
2	0.0000	−0.9354	0.9354	−90.0000	−0.2500

Do you want to plot this?

ZERO LOCATIONS

#	REAL	IMAG	RADIUS	ANGLE	FREQ (FC)
1	0.9792	0.2028	1.0000	11.7000	0.0325
3	0.7785	0.6277	1.0000	38.8800	0.1080
5	0.4258	0.9048	1.0000	64.80000	0.1800
7	−0.4258	0.9048	1.0000	115.2000	0.3200
9	−0.7785	0.6277	1.0000	141.1200	0.3920
11	−0.9792	0.2028	1.0000	168.3000	0.4675

Do you want to plot this?

POLYNOMIAL COEFFICIENTS:

$Z^{**}0$	COEF =	1.00000
$Z^{**}1$	COEF =	0.00000
$Z^{**}2$	COEF =	0.98468
$Z^{**}3$	COEF =	0.00000
$Z^{**}4$	COEF =	0.89773
$Z^{**}5$	COEF =	0.00000
$Z^{**}6$	COEF =	0.97715
$Z^{**}7$	COLF =	0.00001
$Z^{**}8$	COEF =	0.89774
$Z^{**}9$	COEF =	0.00000
$Z^{**}10$	COEF =	0.98467
$Z^{**}11$	COEF =	0.00000
$Z^{**}12$	COEF =	1.00000
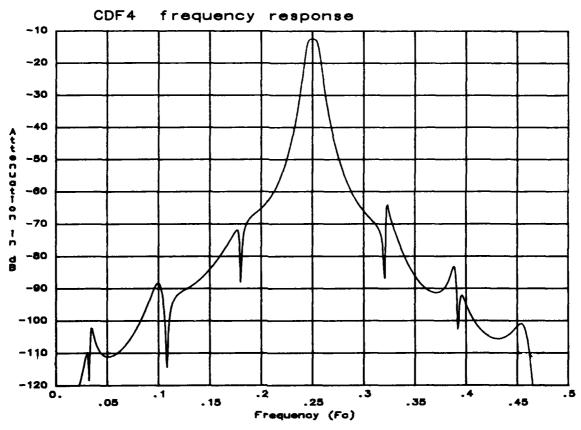
TOTAL RESPONSE
Do you want to plot this?

9.2.3 Chip Design and Experimental Results

The design and layout of the integrated circuit chip which implemented the above design is the next task. All of the internal sections of the filter have been defined. The remaining design questions include the signal input to the chip, (the voltage-to-charge conversion) the output charge-to-voltage conversion, and the connection of the various sections.

The input section uses the fill-and-spill technique. The fill operation is shown if Figure 9.26b with the excess charge spilled out in Figure 9.26c leaving a charge packet whose size depends on the difference in voltage between the reference and input electrode. This charge packet is then available for clocking into the first standard pseudo-one phase stage (Figure 9.26a).

CDF4 frequency response

Figure 9.24. Bandpass filter frequency response.

CDF4 frequency response
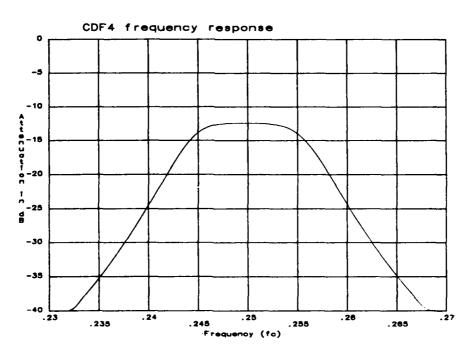
Figure 9.25. Bandpass filter frequency response — expanded view
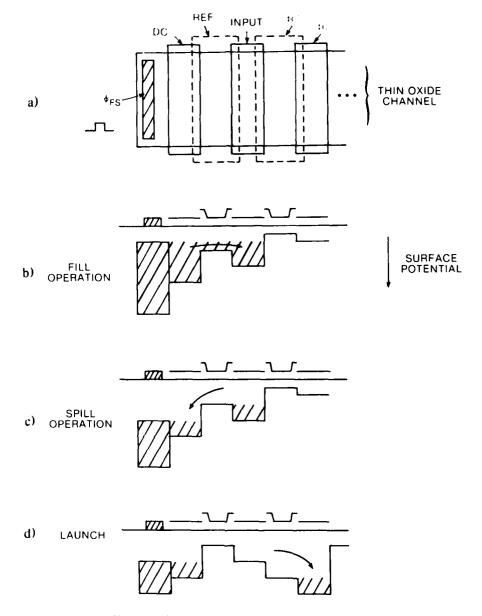
Figure 9.26. Fill and spill charge input circuit.

A reset-and-float diffusion is used as an output circuit with a two stage source follower to drive off-chip electronics or scope probe capacitance. The schematic is shown in Figure 9.27.

The usual technique of connecting isolated sections of a CCD chip, namely using a diffusion at the inputs and outputs of the subsections connected together with a metal line, gives errors in the real pole section of CDF2. These errors are caused by a lack of lateral equilibration of the charge packet prior to the barrier splitting operation. For a pseudo one phase CCD clocking scheme there are two DC gates, a transfer gate and a storage gate. Either or both of these may be sliced into two halves in the direction perpendicular to charge flow in the channel, and a diffused n-type region may be placed in between the two halves in order to enhance the lateral equilibration speed. The diffusion may also have a metal overlaying it to further enhance this speed. This is shown in Figure 9.28 where both the DC transfer and DC storage gates are split. A metalized diffusion may also be placed between the transfer and storage gates, without significantly degrading the transfer speed. The metallized diffusion can actually
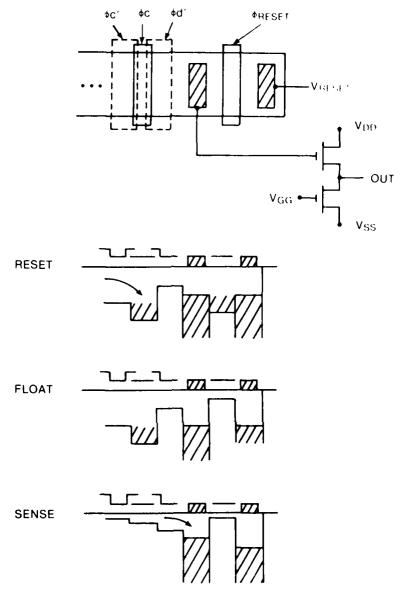
Figure 9.27. Reset and float output circuit.

be two diffused areas connected by the metal, as is done in turnarounds, etc. In previous designs such as CDF2 a single metallized diffusion is used as the interconnection of non-adjacent channels as well as a mechanism for high speed lateral equilibration. This causes the feedback coefficient to be in error.

The new structure which splits both the transfer and storage electrodes separates the functions of connection and lateral equilibration. The connection function is performed by the split transfer electrode. The charge then spills into the split storage electrode so that even if all of the charge is transferred to one end of the storage electrode, once there it will equilibrate along its whole length before being transferred on to the next stage where barrier splitting occurs. This type of interconnect avoids the worries of balancing capacitance and minimizing resistance. This technique is used for connecting all the sections of the bandpass filter. In addition this structure has been tested as a new implementation of the CDI 2 real pole with barrier splitting and simple stage feedback (see Figure 9.29). The accuracy of the real pole coefficient is improved from 1% error to a 0.2% error and shows no significant fluctuation with bias level or clock speed (up to the limits imposed by transfer inefficiency).
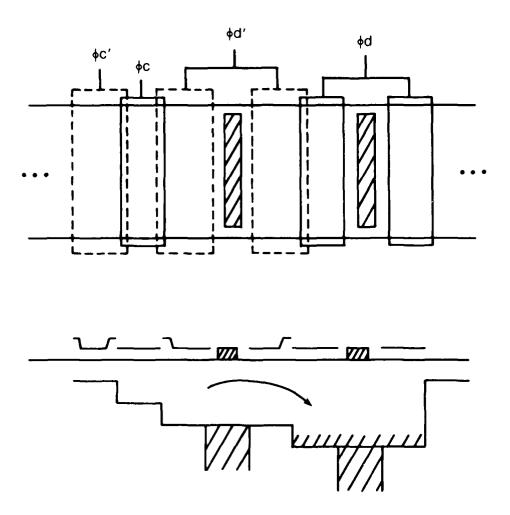
Figure 9.28. CCD structure for enhancing lateral equilibration.

The chip CDF3 has been layed out according to the design considerations discussed above. The chip (Figure 9.30) has been processed with the 6 μm design rule n-channel process as used for CDF2. An additional test chip is included to allow testing of the individual filter sections. The test chip demonstrates proper operation of each of the sections individually, verifying operation of the modified circular shift register as well as the new method of interconnecting filter sections. The impulse response measurements again show accuracy to about 0.2% and the frequency response as measured on a spectrum analyzer agrees with the simulation to better than 0.5 dB from DC up to the Nyquist frequency.

The overall filter, however, does not operate. The problem is due to inadequate handling of the bias charge. While the early stages may attenuate the signal charge level, the bias charge is not attenuated. Later stages must be built to handle the entire 50% of full well (FW) bias charge of the input stage. The overall charge level at the output is

$$Q_{out} = .5\ FW \pm (.5 \times SAF)$$

where SAF is the signal attenuation factor in the passband.

The circuit has been redesigned as CDF4 with several improvements. The chip photo is shown in Figure 9.31. The design has been converted to 4 μm design rules which gate a transfer gate length of 4 μm and storage gate length of 9 μm versus 6 and 10 μm for CDF3. The stages which give no insertion loss (the transversal filter and 90° pole sections) are moved to the front end in order to improve

Figure 9.29. Improved single stage feedback structure.
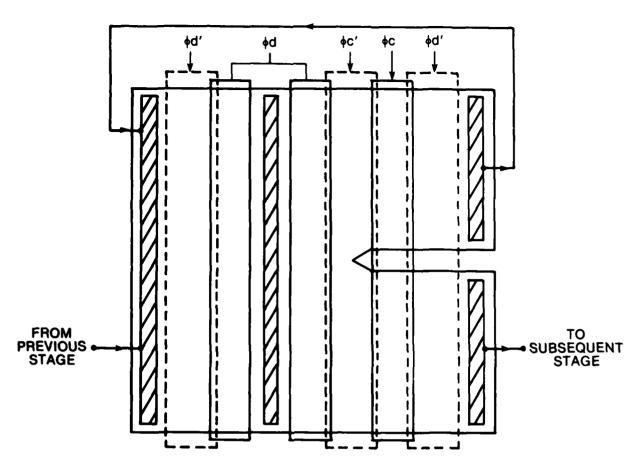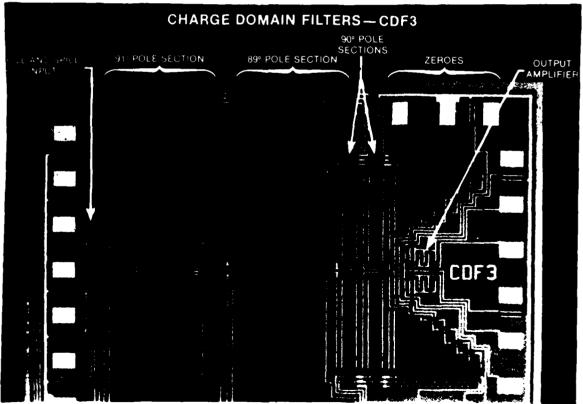

Figure 9.30. Charge domain bandpass filter photomicrograph.
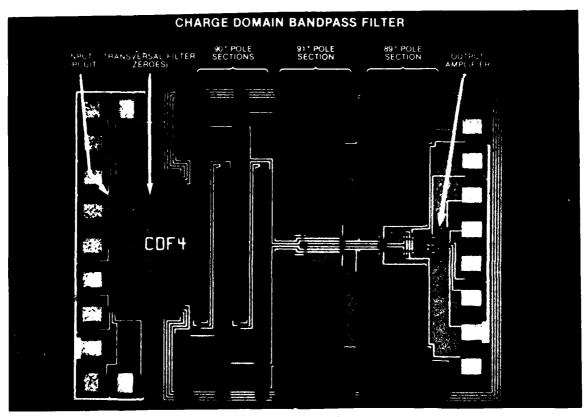
CHARGE DOMAIN BANDPASS FILTER

Figure 9.31. CDF4 bandpass filter photomicrograph.

their accuracy. With this placement scheme, the device handles a greater ratio of signal charge to bias charge, and bias charge variations are not as critical. The input is made directly into the transversal filter section. The channel width is $320 \mu m$, which is the minimum channel width which gives good accuracy in the splitting operation. The next section is a 90° pole pair section. The overall channel width is $1280 \mu m$ with a feedback coefficient of 0.875. The steady state bias handling channel has a width of $(0.125) 1280 \mu m = 160 \mu m$. Thus interposed between the transversal filter section and the 90° pole section is a section which divides the packet into two halves and throws one half away. Following the first 90° pole section is a second 90° pole section. Its output is split in halves with one half directed to the 89° pole section and the other half connected to the 91° pole section. The channel widths of these two sections are $800 \mu m$ with a total feedback coefficient of 0.9. The bias handling channel is $0.1(800) = 80 \mu m$ wide. These two sections have cross-connected inputs to provide the subtraction operation. The outputs are summed together and fed to the output amplifier, a reset-and-float structure with a two stage source follower.

These redesigned chips have been fabricated in General Electric's Corporate Research and Development's semiconductor processing facility. The frequency response of the CDF4 chips as measured on an HP8553A spectrum analyzer is shown in Figure 9.32. Figure 9.33 compares this response to the simulation. The agreement is excellent, with errors less than 1.0 dB outside the noise limited regime. The limit on stopband attenuation of 65 dB is set by device noise rather than by coefficient accuracy. Measured insertion loss is 12.0 dB versus the 12.1 dB predicted. An expanded view of the passband (Figure 9.34) shows good agreement between experimental and theoretical. The experimental results show some extra peaking in the 89° pole compared to the 91° pole. This is caused by a uneven division of the charge which is sent to the 89° and 91° pole sections. Figure 9.35 shows the effect of a 0.5% error in the division into two halves. A redesigned chip should make this split separately from the $1/8 - 7/8$ split used for the 90° pole in order to make the 50% split completely symmetric.
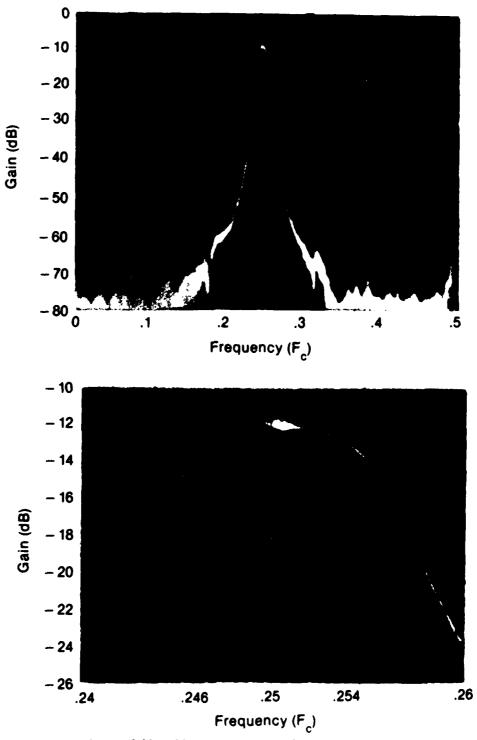
Figure 9.32. CDF4 experimental frequency response.

The demonstration of this filter dramatically shows the unique capabilities of charge domain devices for monolithic signal processing. In addition to demonstrating exceptional frequency response characteristics, this filter verified our simulation tools as well as our capability to determine, in advance, the filter characteristics which can be achieved with the charge domain technique.

9-27

Figure 9.33. Comparison of theoretical (solid) and experimental (dotted) frequency responses for CDF4.

Figure 9.34. Comparison of theoretical (solid) and experimental (dotted) frequency responses for CDF4 — expanded view.

9-28
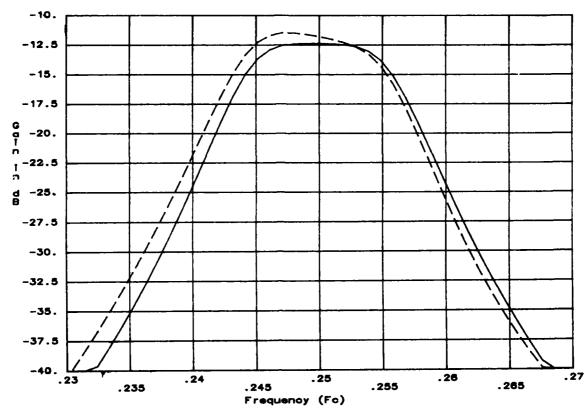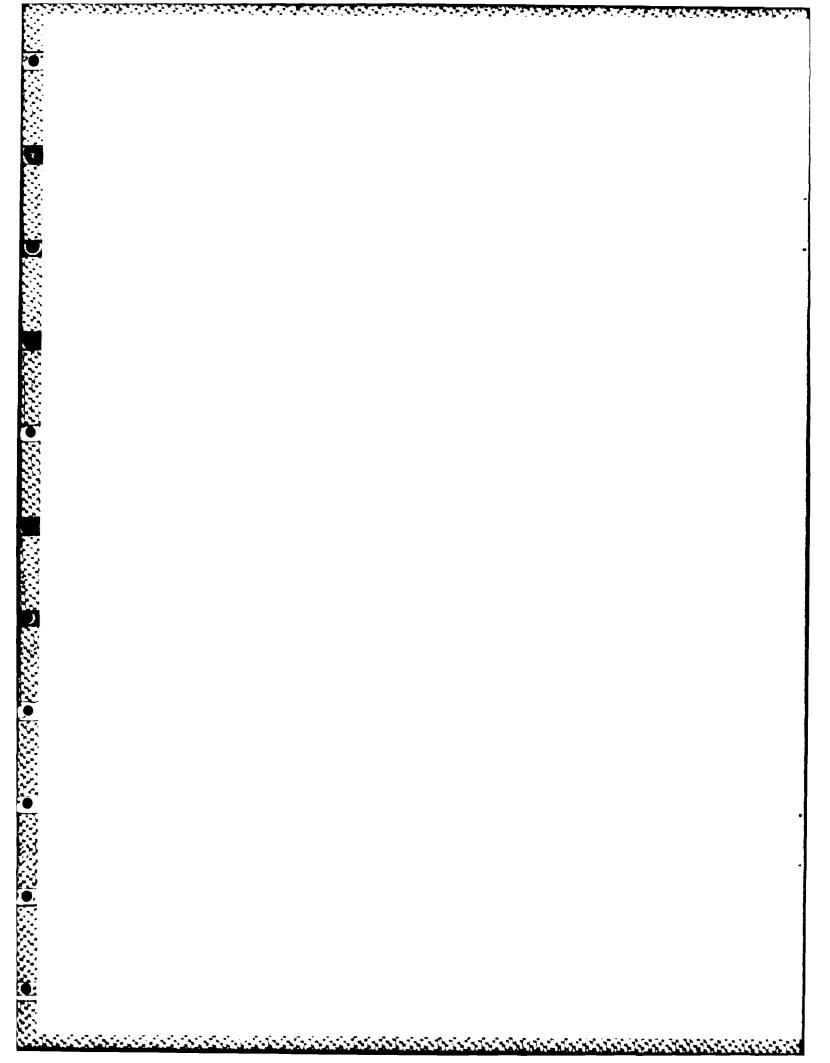
Figure 9.35. The effect of unequal charge packets transferred to the 89° and 91° pole sections on the passband of CDF4 for 0.0% error (solid curve) and 0.5% error (dashed curve).

10. PROGRAMMABLE CDFS

The filters described in the previous section show good performance, but are limited in their flexibility or adaptability since their coefficients and configurations are fixed in their design. It is desirable in many cases to electrically program the filter coefficients or change the filter response after it has been fabricated. A number of techniques have been investigated in order to achieve this goal. Programmable test devices have been fabricated along with the CDF3 and CDF4 filters (see Figure 10.1a). The evaluation of these devices proves that the concepts work as expected. It now appears practical to make a filter which combines the benefits of charge domain signal processing with the flexibility of electrically programming the coefficients. This accomplishment coupled with recent developments in microcomputers and microcontrollers opens up a new realm of possible applications for charge domain signal processing chips.
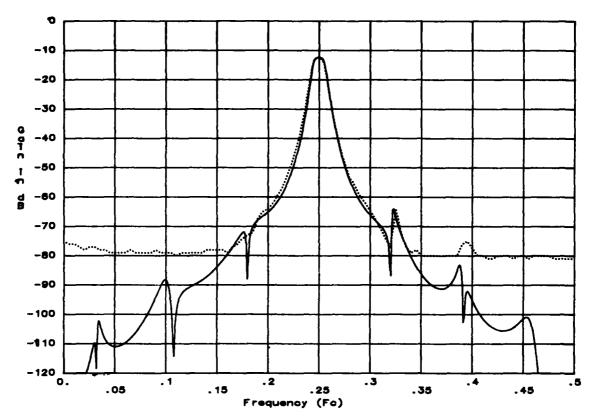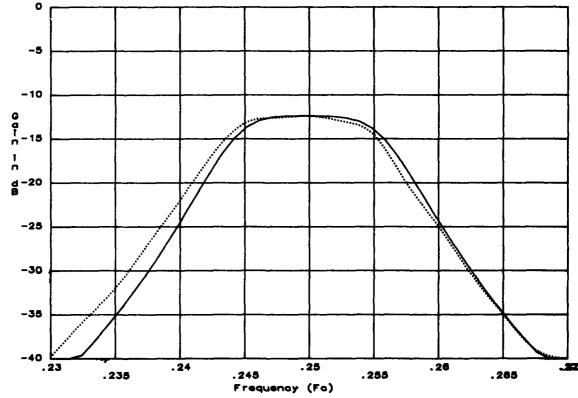
10.1 ALTERNATE PROGRAMMABILITY TECHNIQUES

There are several degrees of programmability which can be incorporated in a CDF design, and in general the more flexible approaches are more costly in terms of chip size, speed, or complexity. The lowest degree of programmability is inherent in any clocked CDF design. The absolute frequency response can be altered just by changing the clocking frequency. A bandpass filter can shift its center frequency in proportion to the clock frequency. The bandwidth, however, also scales with the clock frequency. For some communications systems, where the tuning range is small, this degree of flexibility may be adequate.
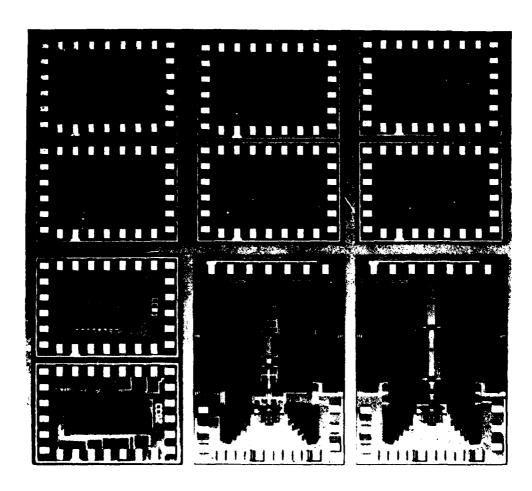
Figure 10.1a.   Charge domain chips including CDF3 filter and PCDF programmable test chips.

The next step up in flexibility is to have a fixed band shape but have independently variable center frequency and bandwidth. An approach which implements this function is the N-path filter shown schematically in Figure 10.2. The commutator at the input demodulates the desired incoming signal frequency down to baseband samples and the commutation speed determines the center frequency. The baseband samples pass through a bank of parallel low pass charge domain filters. The clocking frequency of these filters is used to program the bandwidth. The output of these filters can be synchronously modulated up to the original frequency if desired. Alternatively the baseband signals may be used as outputs. When the number of parallel filters is 4, the baseband signals can be combined to give the in phase (I) and quadrature (Q) outputs directly. This technique has been analyzed to some extent, but most of the efforts in this area have been directed at the next tier of programmability.

The next level up in the programmability chain is the capability of altering the coefficients electrically, but not changing the architecture. The first task is to define programmable charge splitter structures. Three basic structures have been invented and evaluated experimentally. The first is an in-place sequential charge splitter. This approach uses a gated equilibration splitting scheme similar to that used successfully in CDF2. A digital shift register supplies the coefficients, most significant bit (MSB) first.
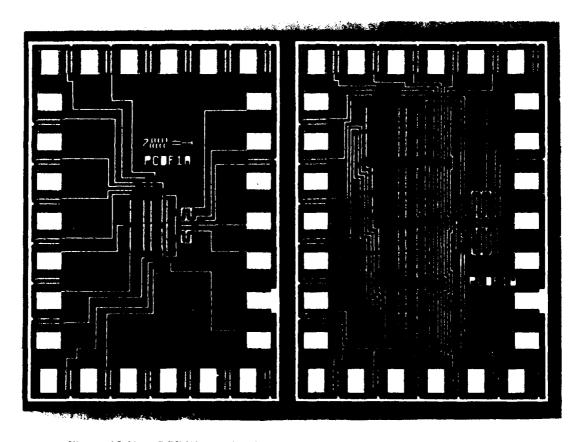
Figure 10.1b.   PCDF1A = in-phase sequential splitter
               PCDF1B = four stage pipe organ filter using sequential splitters.

A schematic diagram of this technique is shown in Figure 10.3. The charge packet is introduced into potential well under the A gate. Meanwhile the B well is empty. At this time the equilibration gate is opened and closed leaving half of the charge packet under A and half under B (note that a splitting ratio of 0.5 simplifies the balancing of the charge splitting mechanism). At this point either the C or D gate is turned on depending on the (MSB), and the 1/2 charge packet is transferred to the E or F accumulator well. Now the A well contains 1/2 the input packet and the B well is empty. The equilibration gate again turns on and off leaving 1/4 of the original packet under A and 1/4 under B. The second bit of the digital coefficient channels the 1/4 under B to the E or F accumulator. The splitting and channeling continues for 1/8, 1/16, etc., for N bits where N is as many bits as is desired. After all the signal (possibly including the leftover $1/2^N$ portion) has been channeled the output can be read out with an overlying electrode (non-destructive readout) and the entire charge packet returned to the A/B reservoir, or with a diode (destructive readout) and a new input sample can be introduced. This technique has the advantages of being compact in size and universal in structure with respect to the number of bits that may be used. Its disadvantage is that the cycle time for a full multiplication is equal to the
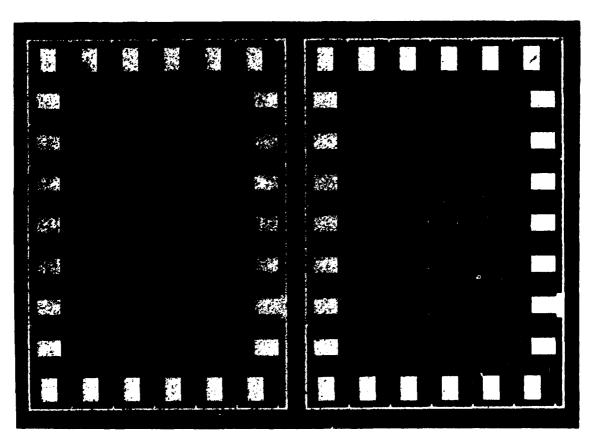
Figure 10.1c.   PCDF1C = four stage split electrode filter using sequential splitters
PCDF1D = flash splitter

clock period of the splitter multiplied by the number of bits. This disadvantage is, however, ameliorated by the high inherent speed of the splitting mechanism.

One of the test devices, PCDF1A (Figure 10.1b) has been used to evaluate this technique. For this and all other PCDF test chips the digital shift registers are off-chip although a production circuit would include on-chip shift registers. The device is operated as a multiplying digital-to-analog converter (MDAC) where the analog input is a DC value and the coefficients are decremented from 127 to 0 (for a 7 bit conversion). The output shown in Figure 10.4 demonstrates excellent linearity over the entire range, with the greatest error at the 64-63 coefficient transition. Seven to eight bits of linear operation have been demonstrated with no degradation at splitting speeds up to 15 MHz. The number of bits is limited by the accurate transfer of charge from the B well to the E or F wells in a short period of time. Structural improvements can yield 9-10 bits of capability.

The second technique overcomes the speed limitations of the sequential splitter at the expense of an increase in chip size. This is the pipelined charge splitter technique diagramed in Figure 10.5. In this case splitting takes place unidirectionally in several stages with each stage providing one binary bit of in-

Figure 10.1d.   PCDF1E = pipeline splitter
                PCDF1F = improved single stage feedback.

Figure 10.2.   N-path filter.

Figure 10.3.   In-place sequential charge splitter.
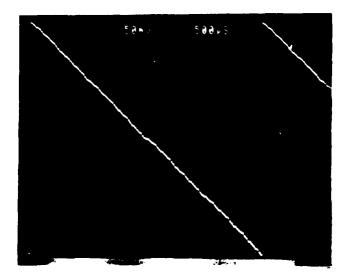
Figure 10.4. In-place sequential charge slitter c   ted as an MDAC.
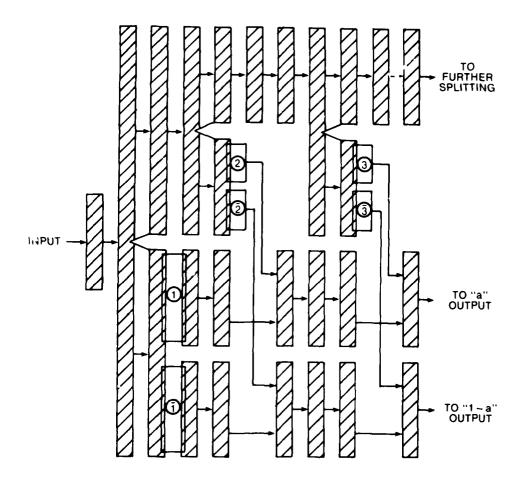
Figure 10.5. Pipelined charge splitter.

creased resolution. The A and $\bar{A}$ accumulators are clocked in synchronism with the splitters such that after 8 clock cycles the product result appears at the output. Due to pipelining the next result appears one cycle later. Therefore the throughput rate of this technique is equal to the clock rate.
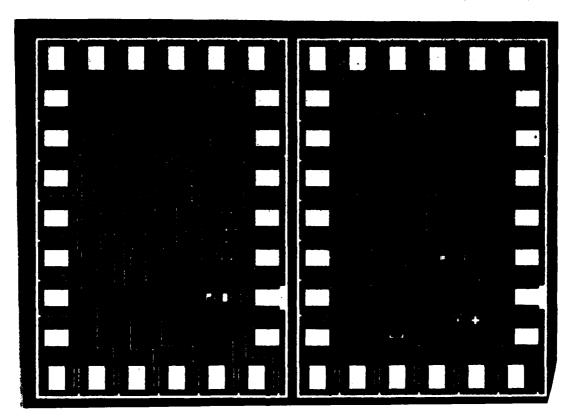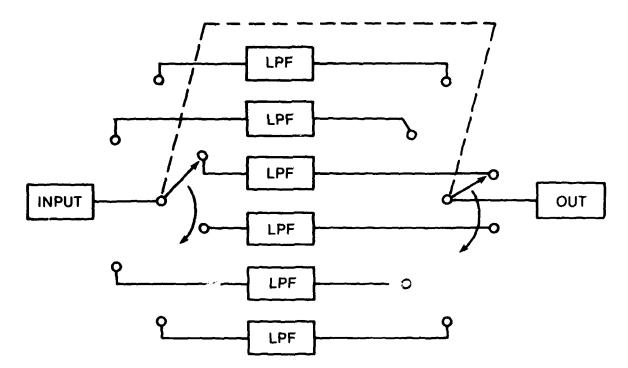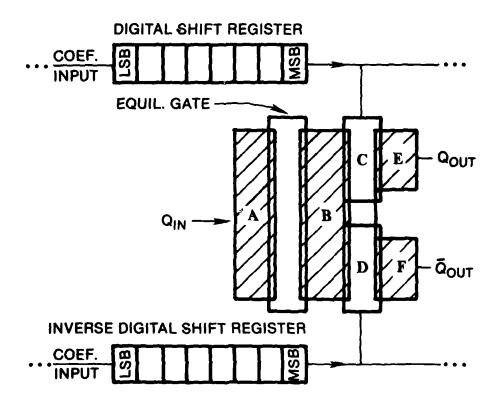
The third approach is a flash splitter. In this approach, shown in Figure 10.6, the channel is simultaneously split into portions equal to 1/2, 1/4, 1/8, . . . 1/2 N and another 1/2 N times the input channel. This approach gives a full n-bit multiplication in one clock cycle. It requires a very wide structure in order to accurately divide the charge.

Both of these concepts have been tested out experimentally. The single bit per stage device, PCDF1E (Figure 10.1d) shows operation as expected, again with 7-8 bits of accuracy in steady state tests. The device is operated as an MDAC with a DC analog input and varying digital coefficients. Unlike the sequential splitter, the accuracy is much poorer than 7-8 bits if the digital coefficient changes from one cycle to the next. This error is caused by the lack of introduction of a fat zero charge into the running accumulators. The high transfer inefficiency results in a large error for the first output value after a coefficient changes. Figure 10.7 shows the results for a constant DC input and eight successive outputs (both plus and minus outputs) for a coefficient of 0, eight outputs for a coefficient of 1, and so on up to a coefficient of 15. Note the error in the first output for each group. This problem is due to high charge transfer inefficiency in the initially empty A and $\bar{A}$ accumulators. This problem can easily be alleviated in future designs by adding a fat zero charge into both accumulators. The four bit flash design PCDF1D (Figure 10.1c) has also been evaluated. It exhibits 6-7 bits of linearity in the MDAC mode (see Figure 10.8). The accuracy appears to be limited by cross coupling of the address lines into the output. Careful shielding and on-chip digital shift registers should alleviate this problem. No transfer inefficiency effects are apparent with this design.
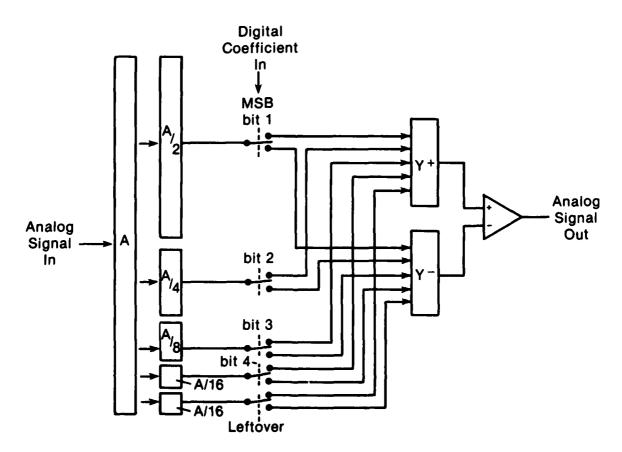
Figure 10.6. Flash charge splitter schematic.
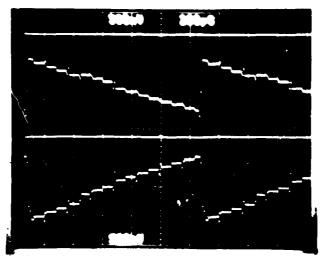
Figure 10.7. Pipelined charge slitter operated as a four-bit MDAC.
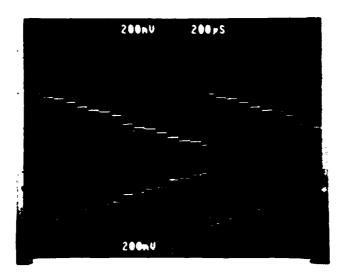
Figure 10.8. Flash charge splitter operated as a four bit MDAC.

The optimum choice for a practical chip may be a hybrid combination of the pipeline and flash approaches. A compact, high speed 9 bit multiplier cell may include three pipelined stages with three bits of flash conversion per stage. This approach appears to be quite practical if careful shielding and proper bias charges are utilized.

The next concern in a circuit implementation is configuration, or how should these programmable coefficient blocks be hooked up. Two representative approaches have been tested. Figure 10.9 is a schematic of a 4-channel pipe organ type connection[12] such as is required for a charge domain programmable transversal filter or charge domain recursive filter section. The test circuit PCDF1B (Figure 10.1b) is such a structure which uses sequential splitters to implement the programmable coefficients. The output of the four channels is summed and sensed with a reset-and-float diffused diode. Each cell operated as described previously with 7-8 bits of linearity with the output equal to the sum of the outputs from each section. The accuracy is good although again better shielding should be incorporated.
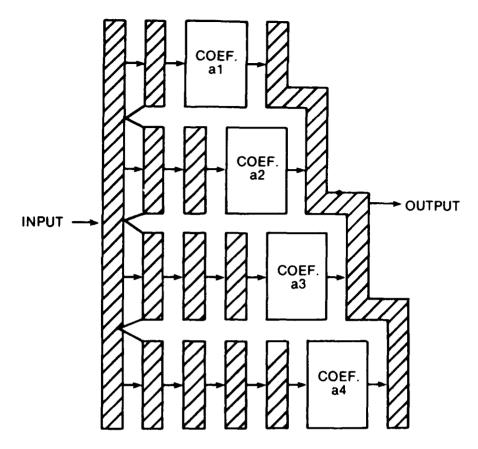
Figure 10.9. Pipe organ type programmable transversal filter.

The alternate circuit configuration, shown in Figure 10.10 is similar to a conventional CCD transversal filter. In this case, a sequential splitter is used to give a programmable tap weight. As in the conventional split electrode filter, the charge is sensed non-destructively on overlying electrodes. Once the charge packet is sensed, it may be transferred on to the next stage. Alternatively, the charge packet may be retained at one site and the digital coefficients may be shifted from one stage to the next, the so-called moving reference structure. The first approach is included as a test chip, PCDFIC, (Figure 10.1c) and operates as expected, the output being the sum of the outputs of the individual cells. The second approach has some inherent advantages over this. First of all, charge transfer inefficiency effects will not degrade performance since the charge packet is retained in a single cell. Secondly, the loading and shifting of the digital coefficient is easier. Third, and most important, is the ability to easily connect up many sections and even many chips in series to obtain very long correlation products or large time-bandwidth products. One such design is discussed in the next section.

Figure 10.10. Split electrode type programmable transversal filter.

11. APPLICATIONS

This contract has addressed the understanding and development of tools for designing CDF's. The next task is to find applications which could utilize charge domain devices to reduce system size, power, and cost and/or improve performance. Several features of CDF's which are important for some applications are discussed, and then several representative applications are detailed.

11.1 FURTHER CAPABILITIES OF CDF'S

In the drive for higher speed monolithic signal processing, several features of charge domain devices become particularly attractive. The first advantage which can be utilized is the higher speed and lower transfer inefficiency of buried channel device fabrication. As discussed earlier, linearity is maintained with buried channel CDF's and their clocking rate is only limited by transfer efficiency effects.

Another feature of CDF's in particular and sampled data systems in general is the use of alias band processing, where the incoming signal frequency is above the device clocking frequency. For instance the bandpass filter CDF4 has its center frequency (f_o) at 1/4 of the clock frequency (F_c). However frequencies of 3/4 F_c, 5/4 F_c, 7/4 F_c or

$$f = nF_c + -f_o \quad n = 0,1,...$$

will also be passed. In addition the sampling operation can be used to down-convert the signal to the $n = 0$ band. Short prefilters can be used to suppress the undesired passbands.

11.2 APPLICATIONS EXAMPLES

One application which can use this technique is shown in Figure 11.1. The primary filter which does the band shaping is the 75 stage filter which is clocked at 20 MHz. It has its passbands at $f = 5, 15, 25, \ldots$ MHz. The CDF4 chip can be used as this filter. Short prefilters can be added on the same chip to suppress those passbands at 5, 15, ... 65, 85, 95, ... i.e., just leaving the 75 MHz passband. The prefilters only require a few charge domain transversal filter stages and therefore require little power
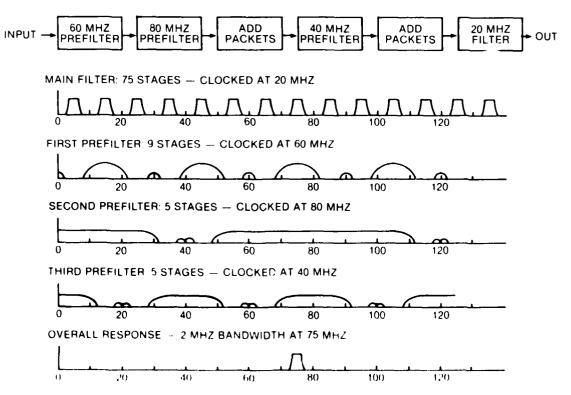

Figure 11.1. 75 MHz if filtering utilizing alias bands and small prefilters.

and are relatively insensitive to transfer inefficiency. By using alias bands and prefilters a high performance low power charge domain filter can be made to operate at very high speeds.

Another application of this technology is to improve performance of conventional CCD split electrode filters. The required zeroes of a transversal filter can be divided between the charge domain section and the split electrode section. Such a structure is diagrammed in Figure 11.2. Oftentimes the filter function can be factored such that the CDF section requires only positive coefficients, further simplifying the operation. One practical application of this technique is to use the higher speed CDF as an anti-alias prefilter (as in the last example) with the lower speed split electrode filter or programmable CDF transversal filter providing the band shaping function.

Another application which uses the alias band processing as well as the demodulation capabilities of the sampling operation is an FM communications system chip. This application has been analyzed recently and a white paper describing the system was submitted in March 1983. This paper is included here as Appendix 4.

Finally a programmable charge domain device has been analyzed using the moving reference architecture with sequential splitters. One hundred stages can be incorporated on a chip. This chip can function as a programmable digital-analog correlator, a programmable or adaptive finite impulse response filter, or a pulse compression filter. Several of these chips can be cascaded for longer correlation products. This chip was described in a white paper report submitted January 1983 and is included here as Appendix 5.

This list of applications is by no means all inclusive; it is only a suggestion of what may now be practical with the demonstration of the capabilities of charge domain. Other application areas for which this technology may be attractive include IF filters, 2D programmable correlators and image processors, steerable radar or sonar beam formers, spread spectrum communication coders and decoders, video filters, FFT's matrix multipliers, D/A converters, A/D converters or any function requiring high data rate sampled data signal processing.
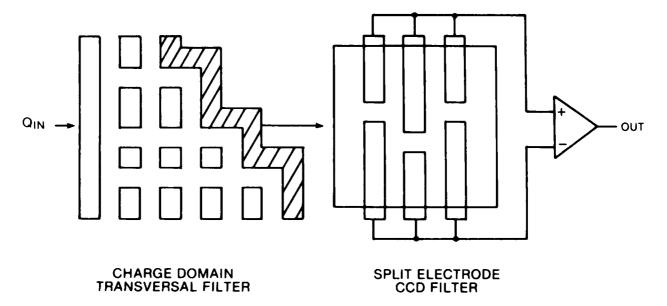

**CHARGE DOMAIN
TRANSVERSAL FILTER**

**SPLIT ELECTRODE
CCD FILTER**
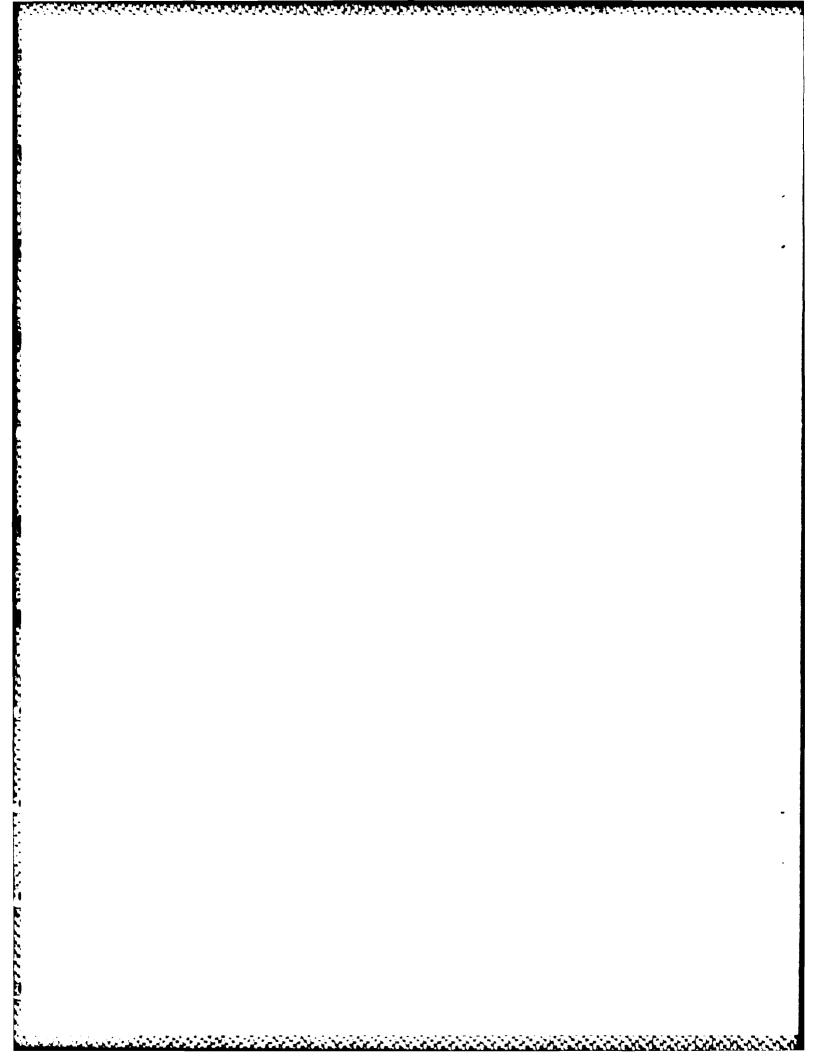
Figure 11.2. CDF/CCD hybrid device.

12. SUMMARY

The contract effort to develop charge domain filters for enhanced monolithic signal processing was quite successful. The first goal of investigation of the capabilities and limitations of these devices was addressed through studies of the charge splitting operation, studies of various specific charge manipulation structures, studies of the use of poles as well as zeroes for implementing transfer functions, and studies of techniques for placing poles and zeroes in the z-plane efficiently under the constraints of the charge domain technology. In addition testing techniques and simulation tools were developed to aid in the design and understanding of operation of charge domain filters.

The second goal of the program was the actual design, layout, and fabrication of a multi-pole filter which would demonstrate the unique capabilities of charge domain technology. A narrowband bandpass filter was investigated as the test vehicle, since it pushed beyond the limits of what was through practical at that point. Several key discoveries permitted this filter to be designed with impressive specifications. The device was fabricated and the demonstrated performance matched the theoretical predictions to a high level of accuracy. A general design methodology for CDF's was developed and expanded which along with the simulation tools permits application to be investigated quickly and practical chips to be designed easily.
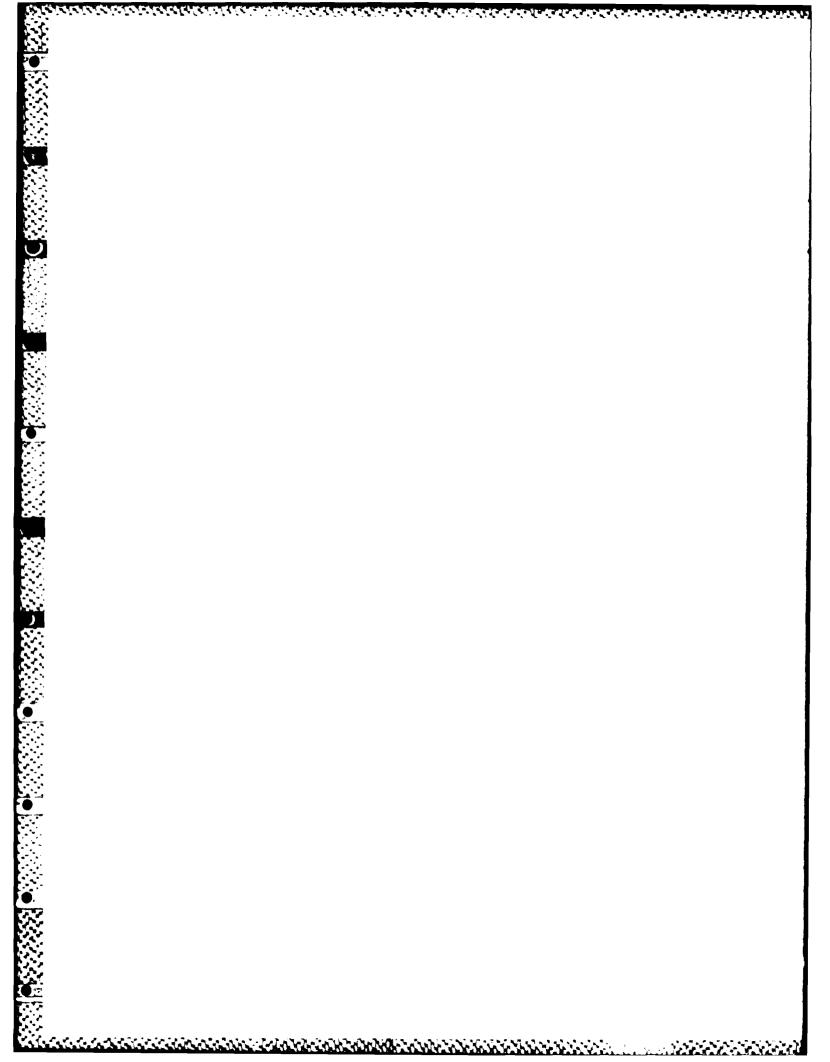
The final goal of the contract was the investigation of techniques which would enable a CDF to be programmed electrically, presumably by a microcomputer in a systems application. A number of levels of programming flexibility were investigated and some concepts were designed in silicon and tested out. These programmable coefficient test blocks and four stage filters successfully demonstrated the ability to provide 7-8 bits of digital coefficient accuracy in the multiplication operation. Large multi-stage chips with 8-10 bits of accuracy appeared to be practical.

Finally a number of applications areas and several specific applications were investigated as potential follow on programs to utilize these capabilities. These ranged from FM filters and demodulators to low power video filters to programmable 1D and 2D correlators/filters. The potential for incorporating high performance high speed systems on a chip utilizing charge domain technology is enormous.
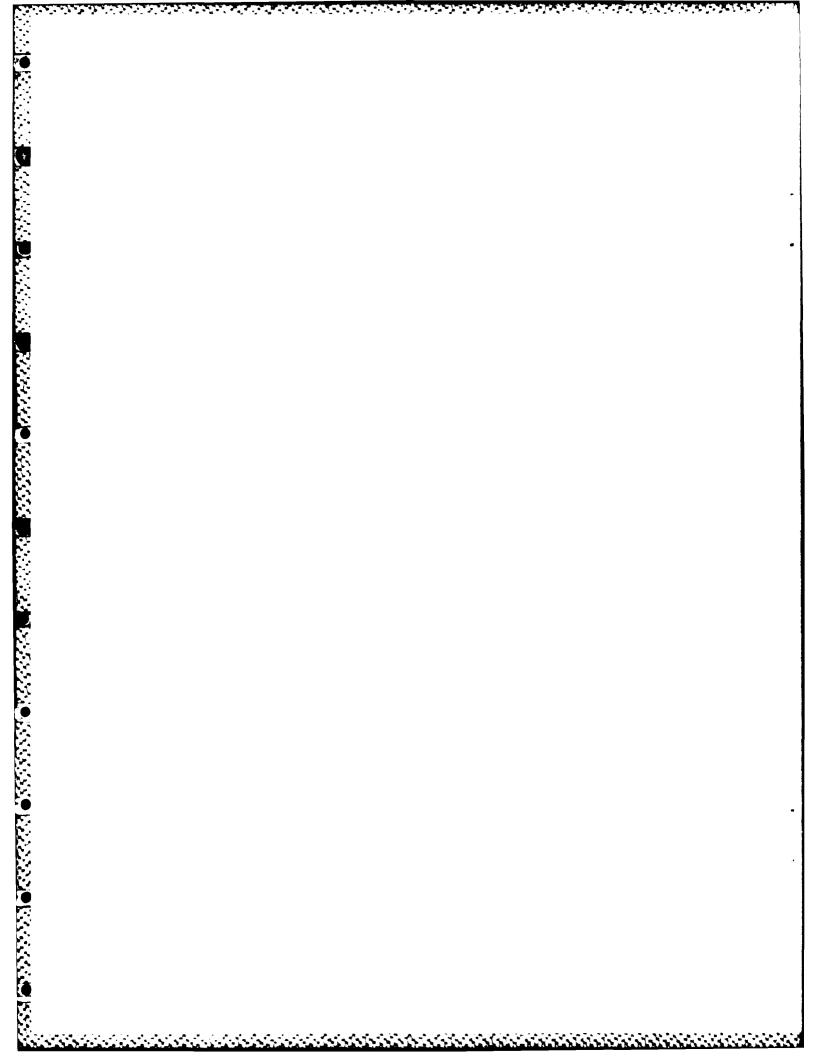
13. ACKNOWLEDGEMENTS

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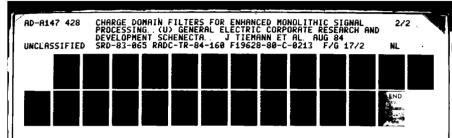
Appendix 1

TIME DOMAIN TYPE TEST PROGRAM

```
10 PRINT:PRINT
15 DEFIN[ A-N:DEPDBL S-T
18 GOTO 1000
20 INPUT 2WHICH PROGRAM 81=CDF2,2=7)"*N
30 ON N GOTO 1000,1000
40 GOTO 2O
1000 REM
1010 REM CDF1 10/26/81
1020 REM
1030 REM THIS PROGRAM CALCULATES AND PRINTS
1040 REM THE IMPULSE RESPONSE OF CDF2
1050 REM
1060 NS=128
1070 DIM X(NS),Y(NS)
1110 INPUT "#READS, # DISPLAYED";NR,NP
1140 SCALE=5/4096
1150 PRINT
1160 PRINT " DATA ","OUTPUT","NOISE","OUTPUT," NOISE "
1170 PRINT "POINT #"," VOLTS","VOLTS","MAXOUT=1","MAXOUT=1"
1170 PRINT "_____","_____"," _____"," _____" ` _____"
1180 MM=H4000
1183 REM GET DATA SUMS
1190 FOR I=1 TO NS
1190 M=H9000+I-1
1193 XA=O:X3=0
1200 FOR J=1 TO NR
1220 A=16*PEE<(M)+PEEK(M+MM)
1222 XA=XA+A
1224 XB=BB+Z*A
1225 4=M+NS
1230 NEXT
1240 X(I)=SCALE*XA/NR
1241 SD=(XB-XA*XA/NR)/(NR-1)
1242 Y(I)=SCALE*SQR(ABS(SD))
1243 OUT 4,I
1250 NEXT
1255 REM SUBTRACT ZERO AND FIND MAX
1260 SX=0:A=0
1270 FOR I=3*NX/4+1 TO NS
1280 SX=SX*X(I)
1290 NEXT
1300 SX=SX/(NS/4)
1310 FOR I=1 TO NO
1320 Z(I)=X(I)-SX
1340 IF ABS(X(I))>YM THEN YM=ABS(X(I))
1350 NEXT
1360 IF YZ=0 THEN YM=100
1370 FOR I=1 TO NP
1380 PRINT I,<(I),Y(I),X(I)/YM,Y(I)/YM
1390 NEXT
1390 PRINT
1390 AS="Y":BS="Y"
```

MICROCOPY RESOLUTION TEST CHART

NATIONAL BUREAU OF STANDARDS .163-A

```
1392 INPUT "RETAKE DATA (Y OR N)";A$
1398 IF A$ = "N" THEN 1110
1400 INPUT "REPEAT CALCULATION (Y OR N)";B$
1410 IF B$ > < "N" THEN 1110
1420 END
```

DIGITAL SIGNAL PROCESSNG ROUTINES

```
C DSP 4/11/83
C
C THIS PROGRAM CALCULATES AND PRINTS AND/OR PLOTS
C THE IMPULSE RESPONSE,FREQUENCY RESPONSE,AND
C POLE-ZERO LOCATIONS FOR A CDF
C GIVEN THE POLE-ZERO LOCATIONS OR
C THE TRANSFER FUNCTION H(Z)
C
C SUBROUTINE LOCATIONS:
C IMSL SBR-ZPOLR(COEF,NDEG,ROOTS,IER)
C 1500 SBR-PZIMP(ZERO,NZERO)
C 1800 SBR-FREQPZ(ZFREQ,NFREQ,ZERO,NZERO)
C 2000 SBR-PZ(POLE,NPOLE,ZERO,NZERO,PCOEF,N,H)
C 2500 SBR-COEF(PCOEF,NPOLE,ZCOEF,NZERO,N,H)
C 3000 SBR-MAG(X,XMAG,XMAGDB,PHI,N)
C 3500 SBR-SAMPLE(XMAG,XMAGDB,PHI,N)
C 4000 SBR-FFT(X,N)
C 4500 SBR-PZMINMAX(POLE,NPOLE,ZERO,NZERO,PCOEF,N,Y)
C 5000 SBR-PRNTIMP(XTIME,NT)
C 5300 SBR-PRNTFREQ(XMAG,XMAGDB,PHI,N)
C 5600 SBR-PRNTPZ(POLE,NPOLE,ZERO,NZERO)
C 6000 SBR-PLTIMP(XTIME,NT,KLAB,SCALE)
C 6300 SBR-PLTMAG(XMAGDB,N,KLAB,SCALE)
C 7000 SBR-PLTPHASE(PHI,N,KLAB,SCALE)
C 7500 SBR-PLT(ARRAY,N,KLAB,SCALE,XMIN,XMAX,XINC,
C          YMIN,YMAX,YNC,XPOINT,YPOINT,NPOINT,KCHAR)
C    NOTE: N=1 FOR IMP; KLAB=NEG FOR PHASE
C    NOTE: SCALE=1. FOR 8X10 PLOT;SCALE=-1. FOR 16X10 PLOT
C    KPEN PICKS THE PEN COLOR
C    KLAB-THOU: 0=ASKS FOR TITLE / 1=AUTOMATIC PLOT
C    KLAB-HUND: 0=NO AXES / KPEN=AXES AND LABELS
C    KLAB-TENS: 0=NO CURVE / KPEN=PLOT CURVE
C    KLAB-ONES: 0=NO POINTS / KPEN=PLOT DATA POINTS
C 9000 SBR-PLTPZ(POLE,NPOLE,ZERO,NZERO,KLAB,SCALE)
C
C*******************************************
C
      SUBROUTINE PZIMP(ZERO,NZERO)
C THIS ROUTINE CONVERTS THE ZERO LOCATIONS
C INTO AN IMPULSE RESPONSE BY MULTIPLYING
C OUT THE NUMERATOR POLYNOMIAL. THE RESULTS
C ARE PRINTED OUT AS POLYNOMIAL COEFFICIENTS.
      COMPLEX ZERO(64)
      DIMENSION ZPOLY(64,3),ZSUM(66),ZTEMP(66)
      K=1
      ZSUM(1)=1.
      DO 90 I=2,NZERO+1
   90 ZSUM(I)=0.
      DO 100 I=1,NZERO
      P=REAL(ZERO(I))
      Q=AIMAG(ZERO(I))
      IF (Q.LT.0.) GO TO 100
```

```
   20 DO 38 I=1,N
      W=2*PI*(I-1)/N
      Z=COS(W)+J*SIN(W)
      HNUM=(1.,0.)
      IF(NZERO.EQ.0) GO TO 34
      DO 33 K=1,NZERO
   33 HNUM=HNUM*(Z-ZERO(K))
      HNUMMAG=SQRT(REAL(HNUM)**2+AIMAG(HNUM)**2)
      IF (HNUMMAG.GT.HMAX) HMAX=HNUMMAG
   34 HDEN=(1.,0.)
      IF(NPOLE.EQ.0) GO TO 38
      DO 36 K=1,NPOLE
   36 HDEN=HDEN*(Z-POLE(K))
   38 H(I)=HNUM/HDEN
      DO 39 I=1,N
   39 H(I)=H(I)/HMAX
      RETURN
      END
C
C*********************************************
C
      SUBROUTINE COEF(PCOEF,NPOLE,ZCOEF,NZERO,N,H)
C THIS ROUTINE CALCULATES THE FREQUENCY
C RESPONSE, H(W), FROM THE TRANSFER FUNCTION
C NUMERATOR AND DENOMINATOR COEFFICIENTS.
      COMPLEX J,Z
      COMPLEX HNUM,HDEN,H(1024)
      DIMENSION PCOEF(64),ZCOEF(64)
      PI=4*ATAN(1.)
      J=(0.,1.)
      C=1.
      IF (NPOLE.EQ.0) GO TO 21
      DO 20 K=2,NPOLE+1
   20 C=C-ABS(PCOEF(K))
   21 DO 28 I=1,N
      W=2*PI*(I-1)/N
      Z=COS(W)+J*SIN(W)
      IF (NZERO.GT.0) GO TO 22
      HNUM=(1.,0.)
      GO TO 24
   22 HNUM=(0.,0.)
      DO 23 K=1,NZERO+1
   23 HNUM=HNUM+ZCOEF(K)*Z**(K-1)
   24 IF (NPOLE.GT.0) GO TO 25
      HDEN=(1.,0.)
      GO TO 28
   25 HDEN=(0.,0.)
      DO 26 K=1,NPOLE+1
   26 HDEN=HDEN+PCOEF(K)*Z**(K-1)
   28 H(I)=C*HNUM/HDEN
      RETURN
      END
C
C*********************************************
C
      SUBROUTINE MAG(X,Y,Z,PHI,N)
```

```fortran
      ZPOLY(K,1) = P**2 + Q**2
      ZPOLY(K,2) = -2.*P
      ZPOLY(K,3) = 1.
      K = K + 1
  100 CONTINUE
      DO 130 I = 1,K-1
      ZTEMP(1) = ZSUM(1)*ZPOLY(I,1)
      ZTEMP(2) = ZSUM(2)*ZPOLY(I,1) + ZSUM(1)*ZPOLY(I,2)
      DO 110 J = 3,2*I+1
  110 ZTEMP(J) = ZSUM(J)*ZPOLY(I,1) + ZSUM(J-1)*ZPOLY(I,2)
     +  + ZSUM(J-2)*ZPOLY(I,3)
      DO 120 L = 1,2*I+1
  120 ZSUM(L) = ZTEMP(L)
  130 CONTINUE
      print *, ' '
      print *, 'POLYNOMIAL COEFICIENTS:'
      DO 30 I = 1,NZERO+1
   30 WRITE (6,40) I-1,ZSUM(I)
   40 FORMAT (1X,'Z**',I2,' COEF =',F9.5)
      print *, ' '
      RETURN
      END
C
C*********************************************
C
      SUBROUTINE FREQPZ(ZFREQ,NFREQ,ZERO,NZERO)
C THIS ROUTINE CONVERTS ZERO LOCATIONS
C STATED AS FRACTIONS OF THE CLOCK FREQUENCY
C TO Z-PLANE ZERO LOCATIONS
C NOTE: THEY MUST BE ON THE UNIT CIRCLE
      COMPLEX ZERO(64)
      DIMENSION ZFREQ(64)
      NZERO = 0
      PI = 4*ATAN(1.)
      DO 10 I = 1,NFREQ
      W = 2*PI*ZFREQ(I)
      NZERO = NZERO + 1
      ZERO(NZERO) = CMPLX(COS(W),SIN(W))
      IF (ABS(SIN(W)).LT.1E-6) GO TO 10
      NZERO = NZERO + 1
      ZERO(NZERO) = CMPLX(COS(W),-SIN(W))
   10 CONTINUE
      RETURN
      END
C
C*********************************************
      SUBROUTINE PZ(POLE,NPOLE,ZERO,NZERO,N,H)
C THIS ROUTINE CALCULATES THE FREQUENCY
C RESPONSE, H(W), FROM THE POLE AND ZERO
C LOCATIONS.
      COMPLEX J,Z
      COMPLEX HNUM,HDEN,H(1024)
      COMPLEX POLE(64),ZERO(64)
      PI = 4*ATAN(1.)
      J = (0.,1.)
      HMAX = 0.
```

```fortran
         J    J K
         K    K/2
         GO TO 6
       7 J=J+K
         PI=4*ATAN(1.)
         DO 30 L=1,M
         LE=2**L
         LE1=LE/2
         U=(1.0,0.0)
         W=CMPLX(COS(PI/FLOAT(LE1)),SIN(PI/FLOAT(LE1)))
         DO 20 J=1,LE1
         DO 10 I=J,N,LE
         IP=I+LE1
         T=X(IP)*U
         X(IP)=X(I)-T
      10 X(I)=X(I)+T
      20 U=U*W
      30 CONTINUE
         RETURN
         END
C
C*****************************************
C
         SUBROUTINE PZMINMAX(POLE,NPOLE,ZERO,NZERO,PCOEF,N,Y)
C THIS ROUTINE PRINTS THE PEAKS AND VALLEYS OF
C THE FREQUENCY RESPONSE FROM THE POLE AND ZERO
C LOCATIONS
         DIMENSION Y(1024)
         DIMENSION PCOEF(64)
         COMPLEX J,Z
         COMPLEX XNUM,XDEN,X
         COMPLEX POLE(64),ZERO(64)
         IRANGE=4
         PI=4*ATAN(1.)
         print *, '   FREQ   ANGLE   MAG      MAGDB'
C
C CALCULATE NORMALIZING COEFFICIENT 'C'
C
         C=1.
         IF (NPOLE.EQ.0) GO TO 8
         DO 6 K=2,NPOLE+1
       6 C=C-ABS(PCOEF(K))
C
C IF MAG IS INCREASING L=1
C IF MAG IS DECREASING L=0
C INITIALLIZE L=2
C
       8 L=2
         DO 90 I=2,N/2
         A=Y(I+1)
         B=Y(I)
         IF (A.GT.B) GO TO 10
         IF (L.EQ.0) GO TO 90
         L=0
         print *, 'MAX'
         GO TO 20
```

A2-4

```
C THIS ROUTINE CALCULATES THE ABSOLUTE
C MAGNITUDE, MAGNITUDE IN DB, AND PHASE OF
C A COMPLEX ARRAY (E.G. FREQUENCY RESPONSE H(W)).
      COMPLEX X(1024)
      DIMENSION Y(1024),Z(1024),PHI(1024)
      PI=4*ATAN(1.)
      DO 50 I=1,N
      XRE=REAL(X(I))
      XIM=AIMAG(X(I))
      Y(I)=SQRT(XRE**2+XIM**2)
      PHI(I)=(180./PI)*ATAN(XIM/XRE)
      IF((XRE.LT.0.).AND.(XIM.LT.0.)) PHI(I)=PHI(I)-180.
      IF((XRE.LT.0.).AND.(XIM.GT.0.)) PHI(I)=PHI(I)+180.
      IF(ABS(Y(I)).LT.1E-6) Y(I)=1E-6
   50 Z(I)=20*ALOG10(Y(I))
      RETURN
      END
C
C*****************************************
C
      SUBROUTINE SAMPLE(Y,Z,PHI,N)
C THIS ROUTINE MODIFIES THE FREQUENCY
C RESPONSE BY SIN X / X FOR SAMPLING AT THE
C CLOCK FREQUENCY
      DIMENSION Y(1024),Z(1024),PHI(1024)
      PI=4*ATAN(1.)
      DO 51 I=2,N/2+1
      XJ=(I-1)*PI/N
      Y(I)=Y(I)*(1-(1.8*(1-SIN(XJ)/XJ)))
   51 Z(I)=20*ALOG10(Y(I))
      RETURN
      END
C
C*****************************************
C
      SUBROUTINE FFT(X,N)
C THIS ROUTINE PERFORMS AN N-POINT FFT ON
C THE COMPLEX ARRAY X, AND RETURNS THE
C RESULT IN X.
      COMPLEX X(1024),U,W,T
      M=0
      NN=N
      DO WHILE (NN.GT.1)
         NN=NN/2
         M=M+1
      END DO
      NV2=N/2
      NM1=N-1
      J=1
      DO 7 I=1,NM1
      IF(I.GE.J) GO TO 5
      T=X(J)
      X(J)=X(I)
      X(I)=T
    5 K=NV2
    6 IF (K.GE.J) GO TO 7
```

```fortran
      10 IF (I.EQ.1) GO TO 90
         I = 1
         print *, 'MIN'
C
C PRINT OUT MAX OR MIN VALUES
C AND VALUES AROUND MAX OR MIN
C
      20 WW = 2*PI*(I-1)/N
         DO 80 IW = -IRANGE,IRANGE
         W = WW + (2*PI*IW)/(N*IRANGE)
         Z = COS(W) + (0.,1.)*SIN(W)
         XNUM = (1.,0.)
         IF (NZERO.EQ.0) GO TO 40
         DO 30 K = 1,NZERO
      30 XNUM = XNUM*(Z-ZERO(K))
      40 XDEN = (1.,0.)
         IF (NPOLE.EQ.0) GO TO 70
         DO 60 K = 1,NPOLE
      60 XDEN = XDEN*(Z-POLE(K))
      70 X = C*XNUM/XDEN
         XRE = REAL(X)
         XIM = AIMAG(X)
         XMAG = SQRT(XRE**2 + XIM**2)
         XMAGDB = 20*ALOG10(XMAG)
      80 WRITE (6,85) W/(2*PI),W*360/(2*PI),XMAG,XMAGDB
      85 FORMAT(F13.4,F9.2,E12.3,F10.3)
      90 CONTINUE
         RETURN
         END
C
C*****************************************
C
      SUBROUTINE PRNTIMP(T,NT)
C THIS ROUTINE PRINTS THE IMPULSE RESPONSE.
      DIMENSION T(1024)
      print *, ' '
      print *, 'IMPULSE RESPONSE:'
      print *, ' '
      WRITE (6,15) (I,T(I),I=1,NT)
      15 FORMAT(I5,F12.5)
      print *, ' '
      RETURN
      END
C
C*****************************************
C
      SUBROUTINE PRNTFREQ(Y,Z,PHI,N)
C THIS ROUTINE PRINTS THE FREQUENCY RESPONSE.
      DIMENSION Y(1024),Z(1024),PHI(1024)
      print *, ' '
      print *, 'FREQUENCY RESPONSE:'
      print *, ' '
      WRITE (6,24)
      24 FORMAT (3X,'#',10X,'MAG',8X,'MAGDB',8X,'PHASE')
      WRITE (6,25) (I,Y(I),Z(I),PHI(I),I=1,N/2+1)
      25 FORMAT (I5,3X,F12.5,3X,F10.3,3X,F10.3)
```

```fortran
      print *,' '
      RETURN
      END
C
C******************************************
C
      SUBROUTINE PRNTPZ(POLE,NPOLE,ZERO,NZERO)
C THIS ROUTINE PRINTS THE POLE AND ZERO
C LOCATIONS IN X-Y AND R-THETA COORDINANTS.
      COMPLEX POLE(64),ZERO(64)
      PI=4*ATAN(1.)
      IF (NPOLE.EQ.0) GO TO 30
      print *,' '
      print *, 'POLE LOCATIONS'
      print *,' #    REAL    IMAG    RADIUS   ANGLE   FREQ(FC)'
      DO 25 I=1,NPOLE
      RADIUS=SQRT(REAL(POLE(I))**2+AIMAG(POLE(I))**2)
      P=REAL(POLE(I))
      Q=AIMAG(POLE(I))
      IF (ABS(P).GT.1E-8) GO TO 15
      ANGLE=90.
      IF (Q.LT.0) ANGLE=-90.
      GO TO 20
15    ANGLE=(180./PI)*ATAN(AIMAG(POLE(I))/REAL(POLE(I)))
      IF ((AIMAG(POLE(I)).GT.0.).AND.(REAL(POLE(I)).LT.0.))
     &ANGLE=ANGLE+180.
      IF ((AIMAG(POLE(I)).LT.0).AND.(REAL(POLE(I)).LT.0.))
     &ANGLE=ANGLE-180.
      IF (ANGLE.LT.-1E-6) GO TO 25
20    WRITE(6,10) I,POLE(I),RADIUS,ANGLE,ANGLE/360.
10    FORMAT(I5,5F10.4)
25    CONTINUE
30    IF (NZERO.EQ.0) RETURN
      print *,' '
      print *, 'ZERO LOCATIONS'
      print *,' #    REAL    IMAG    RADIUS   ANGLE   FREQ(FC)'
      DO 45 I=1,NZERO
      RADIUS=SQRT(REAL(ZERO(I))**2+AIMAG(ZERO(I))**2)
      P=REAL(ZERO(I))
      Q=AIMAG(ZERO(I))
      IF (ABS(P).GT.1E-8) GO TO 35
      ANGLE=90.
      IF(Q.LT.0) ANGLE=-90.
      GO TO 40
35    ANGLE=(180./PI)*ATAN(AIMAG(ZERO(I))/REAL(ZERO(I)))
      IF((AIMAG(ZERO(I)).GT.0.).AND.(REAL(ZERO(I)).LT.0.))
     &ANGLE=ANGLE+180.
      IF((AIMAG(ZERO(I)).LT.0.).AND.(REAL(ZERO(I)).LT.0.))
     &ANGLE=ANGLE-180.
      IF (ANGLE.LT.-1E-6) GO TO 45
40    WRITE (6,10) I,ZERO(I),RADIUS,ANGLE,ANGLE/360.
45    CONTINUE
      print *,' '
      RETURN
      END
```

Appendix 3

BANDPASS FILTER DESIGN PROGRAM
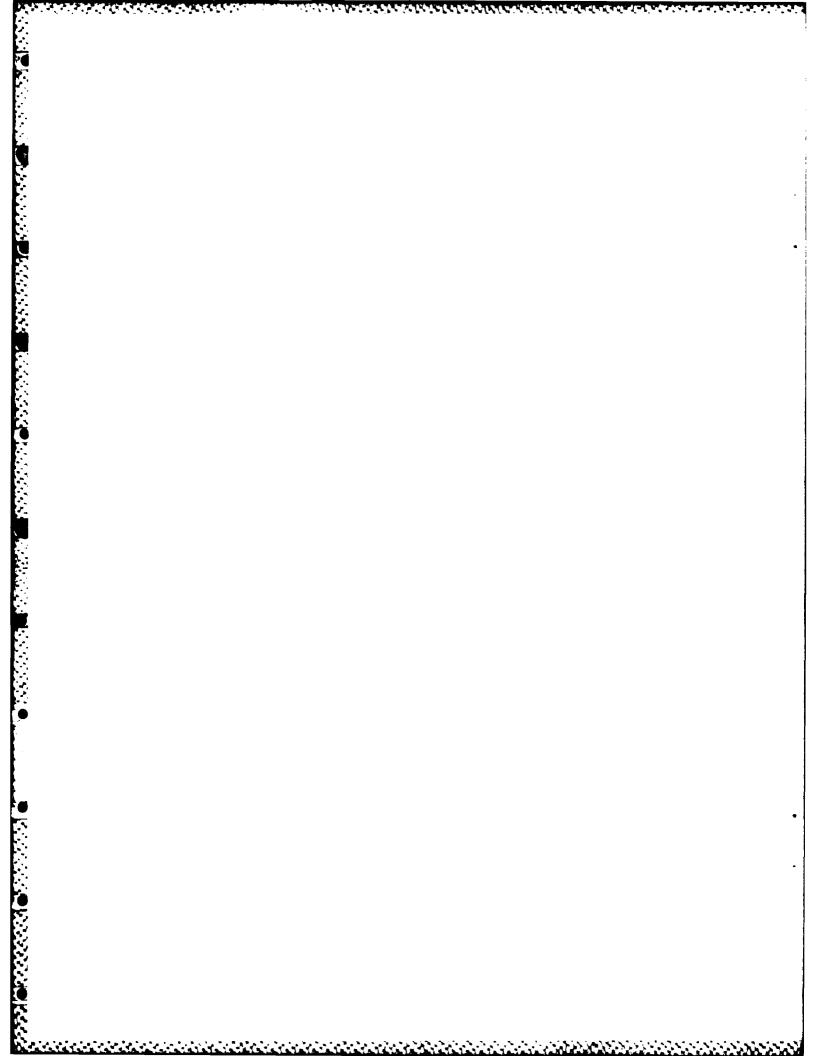
```
c CDF4 5/26/83
c
c This program plots the frequency response for cdf4
c
      COMMON KQUEST,KPRNT,KLAB,SCALE
      COMMON Y(1024),Z(1024),PHI(1024),N,H
      COMMON /ZZZ/PCOEF(64),NPOLE,ZFREQ(64),NFREQ
      COMPLEX G(1024),H(1024)
      DIMENSION XPOINT(64),YPOINT(64)
      PI=4*ATAN(1.)
      M=10
      N=2**M
      SCALE=-1.0
      KPRNT=0
      KQUEST=1
C
C*********************************************
C
      print *, ` `
      print *, 'TITLES'
      DO 8 I=1,N
   8  G(I)=(1.,0.)
      KLAB=100
      CALL PLTPZ(POLE,0,ZERO,0,KLAB,SCALE)
      CALL PLTMG (Z,0,KLAB,SCALE)
C
C*********************************************
C
  10  print *, ` `
      print *, '91 DEG POLES'
      NPOLE=17
      DO 12 I=1,NPOLE+1
  12  PCOEF(I)=0.
      PCOEF(1)=1.
      PCOEF(15)=.6
      PCOEF(18)=.3
      KLAB=30
      CALL CALCPOLE
      DO 14 I=1,N
  14  G(I)=G(I)*H(I)
C
C*********************************************
C
  20  print *, ` `
      print *, '89 DEG POLES'
      NPOLE=19
      DO 22 I=1,NPOLE+1
  22  PCOEF(I)=0.
      PCOEF(1)=1.
      PCOEF(15)=.6
      PCOEF(16)=.1
      PCOEF(20)=.2
```

```
         KLAB=40
         CALL CALCPOLE
         DO 24 I=1,N
  24  G(I) = (G(I)-H(I))
C
C*************************************************
C
  30  print *, ` `
         print *, '90 DEG POLES`
         NPOLE=2
         DO 32 I=1,NPOLE
  32  PCOEF(I)=0.
         PCOEF(1)=1.
         PCOEF(3)=.875
         KLAB=20
         CALL CALCPOLE
         DO 34 I=1,N
  34  G(I)=G(I)*H(I)*H(I)
C
C********************************************
C
  40  print *, ` `
         print *, 'ZEROES`
         NPOLE=0
         NFREQ=6
         DATA (ZFREQ(I),I=1,6) /.0325,.108,.180,.320,.392,.4675/
         KLAB=20
         CALL CALCZERO
         DO 46 I=1,N
  46  G(I)=G(I)*H(I)
C
C*********************************************
C
  50  print *, ` `
         print *, 'TOTAL RESPONSE`
         KLAB=10
         IF (KQUEST.EQ.0) KLAB=KLAB+1000
         CALL MAG(G,Y,Z,PHI,N)
         CALL PLTMG(Z,N,KLAB,SCALE)
  60  STOP
         END
C
C*********************************************
C
         SUBROUTINE PLTMG(Z,N,KLAB,SCALE)
         DIMENSION Z(1024)
         print *, ` `
         print *, 'FREQUENCY RESPONSE PLOT`
         CALL PLT(Z,N,KLAB,SCALE,0.,.5,.1,-80.,0.,20.,0.,0.,0,0)
         RETURN
         END
C
C*********************************************
C
         SUBROUTINE PLTPH(PHI,N,KLAB,SCALE)
         DIMENSION PHI(1024)
```

```fortran
      print *, ' '
      print *, 'PHASE RESPONSE PLOT'
      CALL PLT(PHI,N,-KLAB,SCALE,.22,.28,.01,-180.,180.,90.,0.,0.,0,0)
      RETURN
      END
C
C****************************************
C
      SUBROUTINE CALCPOLE
      COMMON KQUEST,KPRNT,KLAB,SCALE
      COMMON Y(1024),Z(1024),PHI(1024),N,H
      COMMON /ZZZ/PCOEF(64),NPOLE,ZFREQ(64),NFREQ
      COMPLEX H(1024),POLE(64),ZERO(64)
      NZERO=0
      IF (KQUEST.EQ.0) KLAB=KLAB+1000
      CALL ZPOLR(PCOEF,NPOLE,POLE,IER)
      CALL COEF(PCOEF,NPOLE,PCOEF,0,N,H)
      IF (KPRNT.EQ.1) CALL PRNTPZ(POLE,NPOLE,ZERO,NZERO)
      CALL PLTPZ(POLE,NPOLE,ZERO,NZERO,KLAB,SCALE)
      CALL MAG(H,Y,Z,PHI,N)
      CALL PLTMG(Z,N,KLAB,SCALE)
      IF (KPRNT.EQ.2) CALL PZMINMAX(POLE,NPOLE,ZERO,NZERO,PCOEF,N,Y
      RETURN
      END
C
C****************************************
C
      SUBROUTINE CALCZERO
      COMMON KQUEST,KPRNT,KLAB,SCALE
      COMMON Y(1024),Z(1024),PHI(1024),N,H
      COMMON /ZZZ/PCOEF(64),NPOLE,ZFREQ(64),NFREQ
      COMPLEX H(1024),POLE(64),ZERO(64)
      NPOLE=0
      IF (KQUEST.EQ.0) KLAB=KLAB+1000
      CALL FREQPZ(ZFREQ,NFREQ,ZERO,NZERO)
      CALL PZ(POLE,NPOLE,ZERO,NZERO,N,H)
      IF (KPRNT.EQ.1) CALL PRNTPZ(POLE,NPOLE,ZERO,NZERO)
      CALL PLTPZ(POLE,NPOLE,ZERO,NZERO,KLAB,SCALE)
      CALL MAG(H,Y,Z,PHI,N)
      CALL PLTMG(Z,N,KLAB,SCALE)
      IF (KPRNT.EQ.2) CALL PZMINMAX(POLE,NPOLE,ZERO,NZERO,N,Y)
      IF (KPRNT.EQ.1) CALL PZIMP(ZERO,NZERO)
      RETURN
      END
```

Appendix 4

WHITE PAPER

FM DEMODULATION FOR FREQUENCY HOP COMMUNICATIONS SYSTEMS

1. INTRODUCTION

For the past several years, the General Electric Corporate Research and Development Center has been developing Charge Domain Filter (CDF) technology for application to Military Systems needs. (Work performed under contract F19628-80-C-0213.) A CDF is a type of Charge Coupled Device (CCD) for signal processing in which samples of the incoming signal are represented by charge packets which are split up, routed along various paths, and recombined to form new charge packets representing samples of the output signal. All necessary mathematical operations including multiplication, addition and delay can be performed, resulting in a completely flexible signal processing capability. Since all operations are performed directly on the charge packets themselves, non-linearities that commonly arise in charge-to-voltage and voltage-to-charge translations do not occur. These devices are capable of implementing extremely sophisticated signal processing functions with high accuracy, low power, and very high speed. After working out many details of device structure design and filter system architecture, this effort has recently culminated in the design of a bandpass filter with some unusual characteristics. These are illustrated in Figs.1 and 2, which are amplitude plots of the frequency response of the filter. The width of the passband is approximately 1% of the clock frequency, and the pass band has both a linear phase response and a flat amplitude response. The skirt selectivity corresponds to 8 poles, and the stop band drops off to more than -100 dB compared to the passband response. Furthermore, since the insertion loss is only about 12 dB, the dynamic range is expected to be of the order of 70 dB. Since the design is compatible with buried channel CCD structures, it is expected that this filter characteristic can be obtained at any frequency from the audio range up to approximately 100 MHz. Since the center frequency of this filter depends on the clock frequency, it is possible to move its frequency around at electronic speeds. Thus, a filter similar to the one shown could serve as a basis for a highly secure communications system based on frequency hopping.

2. POSSIBLE SYSTEM ARCHITECTURE

A filter such as the one shown can be used in many different applications, and the communications system proposed here is only one suggestion. It was chosen as an example because it exploits a number of the unique characteristics of the CDF filter cited above.

A possible system architecture for a frequency hopping communications system is shown in Fig.3a and 3b. Fig.3a is a schematic system block diagram including a tuner and first i.f. amplifier of conventional design which delivers a relatively broad frequency spectrum and a monolithic "back end" whose function is to select a frequency hopped signal from within the passband of the front end and deliver a fully decoded digital bit stream at its output. Since the monolithic back end is a sampled data system (and therefore has alias passbands), we assume that the passband of the front end is limited to less than one-fourth of the sampling frequency of the monolithic processor. This is indicated in Fig.3b by the dashed line frequency response. In the monolithic processor itself, a first filter is used in one of its alias response bands to select a relatively narrow portion of the spectrum and to down convert it to the fundamental passband of the filter at one-fourth of its clock frequency. This band of frequencies is then further split by a second filter of the same type that is operated at a lower clock frequency. Since this second filter is also operated in an alias passband, a further down conversion is effected, and the bandwidth is further narrowed in the process. Finally, the charge packets are put through a charge domain limiter so as to remove any amplitude modulation that may be present, and is passed to a charge domain FM demodulator which will be discussed further below.

In the above system diagram, it is assumed that all of the operations are performed in the charge domain so that no signal recovery is required at any internal point. The entire system is assumed to be implemented by splitting and recombining of charge packets and by skimming operations. This will

permit a single chip implementation which can operate at high speed with good immunity to power supply variations, etc. In order to accomplish this objective, several of the component subsystems, such as the Charge Domain amplitude limiter and the Charge Domain FM demodulator would need further development effort.

3. PROPOSED RESEARCH PROGRAM

Ideas have already been generated for accomplishing the objective outlined above, and these will now be described.

a. Amplitude limiter.

A method for removing amplitude modulation from a frequency modulated signal is shown in Fig.4a and 4b. Fig. 4a is a surface potential diagram for a new device structure which accomplishes amplitude limiting of an a.c. signal, and Fig.4b is a plan view schematic layout. The operation is based on the principle of skimming.[Ref.] Charge packets representing samples of a sinusoidally varying input signal arrive from the reservoir at the left of Fig.4. and, assuming their amplitude is sufficient to surmount the skimming barrier, they pass over the small output reservoir on their way to the sink. In the process, the output reservoir is filled completely, irrespective of the amplitude of the incoming packet. If, on the other hand, the incoming packet was insufficient to surmount the skimming barrier, no charge at all will enter the output reservoir. Thus, the output reservoir will either be filled completely or totally empty (except, of course for a very narrow range of amplitudes very close to the level of the skimming barrier). If the level of the skimming barrier is adaptively adjusted so that it lies right at the center of the range representing the positive and negative peaks of the input signal, the result will be to turn signals of essentialy any amplitude into square waves of uniform amplitude.

b. FM Demodulator

The demodulator proposed for this system is essentially two frequency sensitive filters, one tuned to the frequency excursion below the carrier, and the other tuned to frequency excursion above the carrier. In order to keep the transient response as short as possible, these filters can be designed as transversal filters with impulse responses that are of finite duration. In practice, filters having impulse responses as short as 9 samples are feasible. Thus, digital bit rates can be as high as one tenth of the clock frequency are possible. These filters can be shaped to produce a linear amplitude versus frequency response in the area of interest as shown in Fig.5. Or, for a digital f.m. demodulation, where only a single frequency shift is present, these filters can be more narrowly tuned and centered on the two shifted frequencies.

4. SUMMARY

Some excellent and unique capabilities possessed by Charge Domain Filters have already been demonstrated, and it is proposed to exploit these in a frequency shift (i.e. FM) digital communications system. This system would be tunable in frequency at electronic speeds, permitting a high speed frequency hop strategy for security and jam resistance. The entire "back end" including second and third i.f., limiter and FM demodulator can be incorporated onto a single silicon chip if desired.

The basic filter technology required—including both device structures and filter system architecture have already been developed, and specific ideas for implementing the limiter and demodulator fuctions have been presented.

Appendix 5

PROGRAMMABLE CHARGE DOMAIN FILTERS FOR SOLID STATE RADARS

1. INTRODUCTION

During the past two years, the General Electric Corporate Research and Development Center has been developing Charge Domain Device (CDD) technology for potential use in military applications. These early developments, while not addressing particular applications, demonstrated that greatly increased linearity and significantly higher clock speed (as compared to conventional techniques) could be achieved by this new technology. The thrust of this work was to improve device operating speed and accuracy and to investigate the underlying device physics which determines the ultimate performance capabilities of this technology. Device simulation tools have been developed to study these new device structures. With the knowledge gained thus far, it is now appropriate to identify some areas of application where CDD's can best be used.

A series of presentations on the subject of CDD capability was recently made to groups of engineers within GE who are involved with military applications. These groups included representatives from G.E.'s Aerospace Electronic Systems Dept., Military Equipment Systems Operation, Ordnance Systems Dept., and other parties knowledgeable in military applications for sophisticated electronic signal processing. One frequently expressed desire was for flexibility, and in particular, for an ability to digitally program the function performed by a signal processing sub-system. Our efforts have correspondingly included the investigation of programmable CDD's, and recent developments have indicated the feasibility of providing this important function in CDD signal processing devices. The discussions also focussed on several specific application areas which are within the reach of present CDD technology, but which are extremely difficult to accomplish by any other means. A building block approach has been conceived which would utilize a chip-cascadable, programmable CDD analog-analog correlator in order to meet the needs of many of these programs.

2. TECHNICAL APPROACH

The technical approach for designing a generic chip which could meet these needs is based on a new signal processing chip architecture which could be called a Moving Reference Programmable CDD. In this architecture, analog samples are scanned into a series of individual programmable charge splitters where they remain until they are replaced. Binary bits representing the K and 1-K coefficients for a tap weight propagate along digital shift registers so that the coefficients move from splitter to splitter in sequence. During each bit time, the charge packet in each of the splitters is split into two equal parts, and the portion corresponding to the binary weight of that bit is delivered to the K or (1-K) accumulator as appropriate. The remaining half is then ready for further binary splitting. When all of the binary bits of a particular tap coefficient have been processed, the output of the entire series is read out by means of a pair of overlying electrodes that sense the charges in the K and 1-K accumulators. After readout, the charges in the K and 1-K accumulators are returned to the same charge splitting reservoir where they started. That is, they are not passed to the next stage as they would be in a conventional CCD filter. At this point, the shift register containing the reference coefficients is clocked so that the binary bits move to the next splitter in the series. The advantages of this architecture include the fact that there is no cumulative charge transfer loss, the digital bits can be passed from chip to chip without degradation, and the output can span several chips, if desired. The lack of charge transfer loss is due to the fact that the analog charge packets do not move from stage to stage. Thus, any charge left behind as a result of charge transfer inefficiency is not mixed with the next sample, but is instead simply recombined with the transferred part of the same sample. The cascading of chips, which is required for the long BT products needed in many applications, is accomplished by simply connecting the shift register outputs from one chip to the inputs of the next and connecting the corresponding overlying electrodes together.

Assuming that 8 to 10 bits of accuracy are needed on the reference coefficients for adequate sidelobe suppression, the splitting clock will have to run at 8 to 10 times the primary sampling rate. This is not a problem however, since the splitting clock on-chip driver would only be driving one low-capacitance electrode. Additional speed may be obtained by implementing the splitting function in buried channel while the output charge sensing procedure (which runs at the sampling rate) could remain surface channel for linearity reasons. Thus sampling rates in the multi-megahertz range are entirely feasible.

3. DISCUSSION

The development of such a correlator chip would provide a practical solution to a broad range of problems including a programmable sampled data filter, a pulse compressor for solid state radars, and a secure communications device, incorporating coded variable analog reference techniques as well as frequency hopping techniques. One particular application which is impractical with conventional technology is outlined below.

At the present time, USAF advanced warning airborne radars utilize high power pulsed klystrons with peak power in the multi-megawatt range in order to provide sensitivity at the desired distances. Not only are these tubes bulky and relatively heavy, but they are also very expensive and difficult to build. A desirable alternative would be an equivalent solid state radar power source, but a direct replacement is out of the question because of the limitations on peak power of solid state devices. Instead, the solid state alternative would use a pulse of longer duration and lower peak power, with appropriate pulse compression to obtain the equivalent peak power. The problem comes about because of the extreme amount of pulse compression required, (namely several thousand to one), the high bandwidth, (namely several MHz.), and the low sidelobe level that can be tolerated. These requirements in combination add up to several giga multiply/add operations per second with at least 12 bits accuracy. Unfortunately, the size and weight of a processor to accomplish this signal processing task is presently at least as large as the klystron it would replace, and the power required would be considerably greater than the transmitter power. By using programmable and cascadable CDD correlators, this task can be accomplished with perhaps a few dozen low power chips.

The alternative of addressing this application with conventional CCD's is not an attractive one. If surface channel CCD's were used, charge transfer losses would be prohibitive. Even buried channel devices become marginal after so many stages, but these could be made to work if a dummy stage (with bias charge only) were inserted between each signal sample. This means that the clock rate would have to be double the sample rate, implying clock rates as high as 10 MHz. in some cases. The number of stages is also doubled, of course, so the power is increased fourfold. We would end up with a CCD with about 5000 stages (10,000 transfers) being clocked at 10 MHz. To avoid transfer loss problems, a CCD of this length and speed would have to be a buried channel device, but this would imply a high degree of output non-linearity. In other words, this application is not well suited to any previously proposed technology--either digital or analog.

4. CONCLUSION

The development of Charge Domain Devices has reached the stage where they may be used in applications to overcome problems that are extremely cumbersome, if not insoluble, with conventional techniques. One particular application which exemplifies this is pulse compression for solid state long range radars. The high speed and programmability capabilities of CDD's provide an attractive solution to this problem. A follow-on program of approximately 18 months total duration to develop this application would be appropriate at this time.

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